International Journal of Research Publication and Reviews

Journal homepage: www.ijrpr.com ISSN 2582-7421

Thyristor Binary Switched Reactor for Voltage Regulation and Reactive Power Compensation Hardware Design

Ashish A.Patil[1], *S.G.Kanade*[2], *Ashish P. Kinge*[3]

[1]M.E.Student,TSSM"S,BSCOER,Narhe,Pune,India
[2]Assistant Professor,Department of Electrical Engineering, TSSM"S, BSCOER, Narhe, Pune, India
[3]Assistant Professor , Department of Electrical Engineering, TSSM"S, BSCOER, Narhe, Pune, India

A B S T R A C T

Topology for reactive power compensation suitable for dynamic loads in closed loop is presented. The scheme consists of Thyristor Binary Switched Reactor (TBSR) banks. TBSR is based on a chain of Thyristor Switched Reactor (TSR) banks arranged in binary sequential manner. A transient free switching of TBSRs is carried out. Proposed topology allows step less reactive power compensation for dynamic loads in very fast responding closed loop.

A topology using a TBSR has been presented. The TSR bank step values are chosen in binary sequence weights to make the resolution small. Current flowing through TBSR as well as source is transient free. Harmonic content in source current is negligibly small. By coordinating the control of TBSR, it is possible to obtain fully step less control of reactive power. Proposed topology can compensate for rapid variation in reactive power on cycle to cycle basis. An attempt is made through this work to develop a scheme with thyristors to reduce the cost by avoiding IGBT‘s and IGCT‘s, technically sound with reliable performance during both steady state and transient conditions, suitable for rapidly changing / fluctuating loads such as arc furnaces, tractions loads, welding equipment's etc., and self-regulating operations are practically both transient and harmonics free. The scheme developed is most suitable for highly nonlinear, fluctuating and harmonic generating loads.

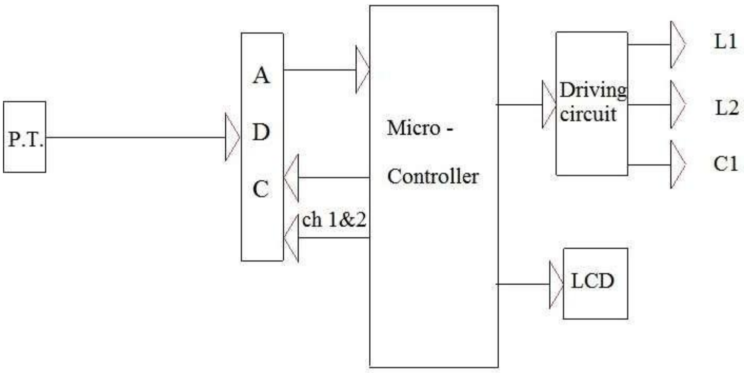
Keywords: Inductive Coil, Thyristor Circuits,Capacitors Transformer,Controller

1.Introduction:

The aggregate behavior of typical load at a substation / on a distribution transformer is somewhat unpredictable since the load changes in its nature, composition, and magnitude from time to time during the day.A comprehensive microcontroller is designed & developed for analyzing the performance of FC-TBSR Compensator. The TBSR consists of reactor bank in two binary sequential steps being operated. It is an error adaptive controller based on voltage sensing for switched capacitor & reactor bank operation. The logic and control techniques employed are unique and comprehensive incorporating number of features. This chapter deals with practical performance evaluation prior to verification with the experimental setup (prototype hardware model) on 1phase, 230volt, 50Hz, AC supply.

2 Block Diagram and Component Description:

The below fig. 5.1 shows the Block Diagram of prototype hardware model of FC- TBSR Compensator with the various components for load voltage sensing and control, used in the controller. It includes load voltage sensing (PT), ADC converter, zero crossing detectors, and gate pulse generation for FC-TBSR bank to ON/OFF bank with the help of microcontroller89C52.



a) Load voltage Sensor(PT):

With the help of PT, load voltage will be measured. The procedure load voltage measured.

Measure voltage at current zero instant, then weget;

- Vm sin (Ø).

This method is very simple and less time consuming as compare with other method. The load voltage and ref voltage compare with help comparator, and given to the comparator.

b) Reactor bankarrangement:

To get the binary values of the reactor is very difficult so to bring the reactor in series-parallel combination. The four reactor bank used as one binary reactor (L1) and three reactor are used as second binary reactor (L2).

Rating of reactor

V=250 V, I=0.4 A, P=40W

Calculation of Reactor:

I.To calculate inductive reactance(XL):

$$I = \frac{V}{XL}$$

$$0.4 = \frac{250}{XL}$$

$$XL = 250 \times 0.4$$

$$XL = 100\Omega$$

$$XL = 2\pi FL$$

$$100 = 2\pi FL$$

$$L = \frac{100}{2\pi \times 50}$$

$$L = 0.3183H$$

To calculate Inductance(L):

I. Total Seven Reactor Bank Are Used To Calculate the Total Inductance andReactive Power

i) First Bank is Series Connected Four Reactor Bank:

$$LS = L1 + L2 + L3 + L4$$

$$= 0.3183 + 0.3183 + 0.3183 + 0.3183$$

$$= 1.27H$$

$$XL = 2\pi \times 50 \times L$$

$$= 2\pi \times 50 \times 1.2732$$

$$= 398.98\Omega$$

$$QL = \frac{V^2}{XL}$$

$$QL = \frac{250^2}{398.98}$$

$$QL = 156.64VAR$$

ii) Second Bank is Series Connected Three ReactorBank:

$$XL = 2\pi \times 50 \times L$$

$$LS = L1 + L2 + L3$$

$$= 2\pi \times 50 \times 0.9549$$

$$= 0.3183 + 0.3183 + 0.3183$$

$$= 99.9968\Omega$$

$$= 0.9549H$$

$$QL = \frac{V^2}{XL}$$

$$QL = \frac{250^2}{99.9968}$$

I. Total reactive power provided by rector bank(Q):

$$Q1 + Q2 = 156.64\ VAR + 625.020VAR$$

$$QT = 781.66VAR$$

i) Capacitive Reactance (XC):

$$XC = \frac{1}{2\pi FC}$$

$$= \frac{1}{2\pi \times 50 \times 5 \times 10^{-6}}$$

$$= 636.619\ \Omega$$

$$QC = \frac{V^2}{XC}$$

$$QC = \frac{250^2}{636.619}$$

$$= 98.17VAR$$

ii) Capacitive Reactive Power (QC):

3 Control Strategy:

The objective here is to maintain load voltage close to specific voltage level (230 V), for all load levels during the day. The reactor bank in two binary sequential steps where operated it is possible to get almost stepless variation of reactive power. The voltages is sensed and fed to a dedicated microcontroller to perform necessary calculations and arrive at the number of steps operation. Control Strategy for Switching of TBSRBank:

In this project we are chosen Reactor bank in binary sequence and also its switching operation is in the form of binary sequence. In fig. 5.7 shows the switch strategy for TBSR bank.

Table 5.1 Switching Strategy

Sr. No.	L1 (Bank)	L2 (Bank)	C1 (Bank)	Load Demand (VL) inVolts
1.	**ON**	**ON**	OFF	550 & above
2.	OFF	**ON**	OFF	550-450
3.	**ON**	OFF	OFF	450-350
4.	**ON**	OFF	OFF	350-300
5.	OFF	OFF	OFF	250-200
6.	OFF	OFF	**ON**	200 below

The total rective power getting from reactor bank is 0 – 780 VAR.The switching of reactor bank in binary sequential manner and corresponding signal that are given from controller to the thyristor are as follows

4Experimental Results:

All the above components are fabricated, tested and implemented as a prototype hardware model, at 230 volts, 50Hz, 1phase AC supply. The load was selected purely resistive and increased from 15W to 75W. The details of the system performance with and without TBSR Compensator are given in the Table 5.2 and Table 5.3respectively.

Performance without TBSC Compensator:

Sr. No.	Load Bank Status	Voltage (V)	Current (A)	Active Power (KW)	Reactive Power (KVAR)	Apparent Power (KVA)	Power Factor (p.f)
1.	No load	542.8	0.8	0.1	0.2	0.2	0.5
2.	One Load On	471.1	1	0.3	0.2	0.3	0.84
3.	Two Load On	318.6	1	0.5	0.2	0.5	0.94
4.	Three Load On	276.1	2	0.5	0.2	0.5	0.93
5.	Four Load On	210.6	2	0.4	0.1	0.4	0.97
6.	Five Load On	92.5	2	0.2	0.1	0.2	0.98

Table 5.3 Sytem Performance with TBSC Compensator:

Sr. No.	Load Bank Status	Voltage (V)	Current (A)	Active Power (KW)	Reactive Power (KVAR)	Apparent Power (KVA)	PowerFactor (p.f)
1.	No load	284	0.8	0.1	0.1	0.1	0.5
2.	One Load On	248.9	1	0.1	0.1	0.1	0.85
3.	Two Load On	209.4	1	0.1	0.1	0.2	0.94
4.	Three Load On	220.2	1	0.3	0.1	0.3	0.99
5.	Four Load On	215.0	2	0.4	0.1	0.4	0.99
6.	Five Load On	191.1	2	0.4	0.1	0.4	0.98

References

1) M. A. EI Sharkawi, S. S. Vankuta, G. Andexler, Mingliangchen and Tony Huang, “Reactive Power Compensation”, us patent No. 5, 134, 356 July 28, 1992.
2) Maffrand, J. W. Dixon, and L. Morán, “Binary controlled, static VAR compensator, based on electronically switched capacitors,” in Proc. IEEE PESC’98, pp.1392–1396, 1998.
3) Juan Dixon, Yamilledel Valle, et al.: A Full Compensating System for General Loads,Based on a Combination of Thyristor Binary Compensator, and a PWM-IGBT ActivePower Filter, IEEE Trans. Industrial Electronics, vol. 50, no. 5,pp. 982- 989.(2003)
4) Juan Dixon, Luis Morán, José Rodríguez, Ricardo Domke, “Reactive PowerCompensation Technologies, State of- the-Art Review”, proceedings of the IEEE, vol. 93,no.12, pp. 2144- 2164, 2005