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H-Bridge Inverter Cascaded with Nested Developed H-Bridge Inverter

Dr.S.Prabakaran[a*], Dr.T.Annamalai[b], S.Anitha[c]

[a]Associate Professor, Department of EEE, SCSVMV University, Enathur, Tamilnadu, India*
[b,c]Department of EEE, Sri venkateswara college of engineering, Sriperumbudur,India

A B S T R A C T

In this paper, a Nested Developed H-Bridge(NDHB) is cascaded with a conventional H-Bridge (HB) inverter to obtain higher-level output voltage. In comparison with the various existing cascaded multilevel inverter topologies, the proposed inverter is able to generate a high number of output voltage levels by using a lower number of power electronic devices such as power switches, driver circuits, power diodes, and DC voltage sources. In addition, the proposed inverter leads to a reduction in installation space and cost of the inverter. As the number of levels increases, the Total Harmonic Distortion (THD) is reduced. This multilevel inverter simulation is done using MATLAB (R2013a).

Keywords:Keywords: Cascaded Multilevel inverter, Nested Developed H Bridge, THD.

1. Introduction

The DC to AC Multilevel Inverter (MLI) eliminates the need for a step-up transformer and can minimize the harmonics produced by the inverter. A cascaded MLI consists of a series of full H Bridges (HB) with isolated DC sources and power switches, and the AC output voltage of each inverter is connected in series to get a cascaded stepped output voltage with increased levels. The major objective of a cascaded MLI topology is to reduce the output voltage harmonic content, to eliminate the electromagnetic interference (EMI) generation elements like inductor and capacitor.The Cascaded H bridge topology can be suitable to generate higher voltage levels because it requires fewer components compared to the conventional topologies [1,2]. Cascaded HB inverters can increase the number of output voltage levels by increasing the number of H-Bridges used, which increases the number of switching devices used; this makes a multilevel inverter more complicated. Modifications to the H-Bridge inverter topology reduces the number of components. A bi-directional power switch is included in the basic H-Bridge to get two extra voltage levels via a capacitor from a single DC input voltage source, and the final output is a stepped five-level output voltage [3–5].The developed H Bridge inverter topology based inverter have been discussed to get more levels with reduced sources and less number of switches compared with symmetrical CHB [6-8]. A new topology developed based on DHB have been discussed with less number of switches being in active 'ON' conduction during all the modes of operation [9-11]. In this paper to double the output voltage levels, the NDHB is cascaded with an HB inverter and reduces the THD.

2. Proposed Technology

The proposed topology is mainly aimed at increasing the number of output voltage levels with reduced THD. The proposed topology produces sixty-three levels at the output with 14 power switches and 5 voltage sources. The proposed topology consists of two units that are cascaded to give sixty-three levels at the output. The two units are a developed H bridge multilevel inverter and a conventional H bridge multilevel inverter. The nested developed H bridge multilevel inverter unit produces 31 levels at the output which when cascaded with a conventional H bridge multilevel inverter produces the desired

* *Corresponding author.*
E-mail address: prabakaran110768@gmail.com

levels at the output.

The NDHB-MLI unit has 10 power switches and 4 DC Input voltage sources with each leg having one voltage source. If the power switches in the same leg turn ON simultaneously, then the DC voltage sources will be short-circuited. Therefore, simultaneous turn ON of power switches in the same leg should be avoided.

The conventional H bridge multilevel inverter unit has 4 power switches and one voltage source. In this conventional H bridge multilevel inverter also simultaneous turn ON of power switches in the same leg should be avoided.

3. Circuit Diagram

The Fig. 1 shows the proposed NDHB cascaded with an H bridge inverter circuit diagram. In this topology, a DHB consists of two half H bridges($V_{L,1}$, $S_{L,1}$ $S_{L,2}$ and $V_{R,1}$, $S_{R,1}$ $S_{R,2}$). The NDHB has the inner DHB nested within another DHB ($V_{L,2}$, $S_{L,3}$ $S_{L,4}$ and $V_{R,2}$, $S_{R,3}$ $S_{R,4}$). The half-bridge of the left-hand side and the right-hand side is cascaded with two unidirectional power switches (S_a, S_b). Finally, the NDHB is cascaded with a conventional H bridge (V_H, S_{H1}, S_{H2}, S_{H3}, S_{H4}) through the load.

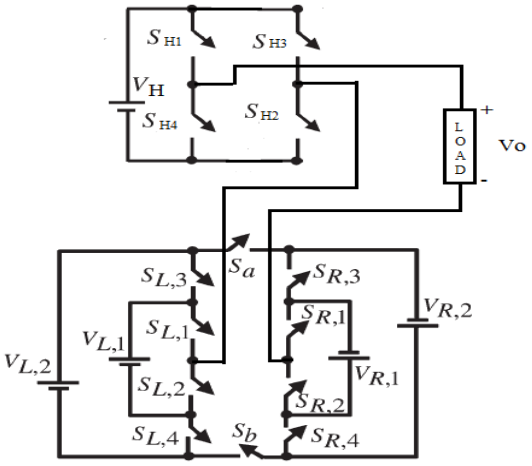

Fig. 1. Proposed Cascaded MLI

To get more number of levels at the output with the reduced number of switches, the magnitude of the DC voltage sources should be different. The magnitudes of the DC voltage sources for the proposed topology is based on the following algorithm,

In this topology, the number of input DC sources ($N_{IN\text{-}source}$) needed to produce the output voltage levels, number of output voltage levels of the NDHB ($N_{OP\text{-}Level\_Nested}$), number of overall output voltage levels ($N_{Overall\text{-}op\text{-}Level}$) are given from Equation (1) to (8).

Design Equation

$V_{L1}=1V_{dc}$ (1)

$V_{R1}=2V_{dc}$ (2)

$V_{L2}=5V_{dc}$ (3)

$V_{R2}=20V_{dc}$ (4)

$V_H=0.5V_{dc}$ (5)

$$N_{IN-source} = n + 1 \quad (6)$$

$$N_{OP-Level\_Nested} = \left[\frac{2[V_{L,n/2}+V_{R,n/2}]}{V_{L,1}} + 1\right] \quad (7)$$

$$N_{Overall-op-Level} = 2\left[\frac{2[V_{L,n/2}+V_{R,n/2}]}{V_{L,1}} + 1\right] + 1 \quad (8)$$

Where,

'n'- Number of DC Sources in the NDHB.

Voltage Levels and its Switching Patterns

The output levels and various switching pattern of the switches used in the topology is given in the following table. In this table '1' indicates the switch is ON and '0' indicates the switch is OFF.

Table 1 switching pattern of proposed cascaded Multilevel Inverter

S NO	S_{L1}	S_{L2}	S_{L3}	S_{L4}	S_{R1}	S_{R2}	S_{R3}	S_{R4}	S_{H1}	S_{H2}	S_{H3}	S_{H4}	S_a	S_b	Vo
1	1	0	1	0	1	0	1	0	1	0	0	1	0	1	$V_{L2}+V_{R2}+V_H$
2	1	0	1	0	1	0	1	0	0	1	0	1	0	1	$V_{L2}+V_{R2}$
3	0	1	1	0	1	0	1	0	1	0	0	1	0	1	$V_{L2}+V_{R2}+V_H-V_{L1}$
4	0	1	1	0	1	0	1	0	0	1	0	1	0	1	$V_{L2}+V_{R2}-V_{L1}$
5	1	0	1	0	0	1	1	0	1	0	0	1	0	1	$V_{L2}+V_{R2}+V_H-V_{R1}$
6	1	0	1	0	0	1	1	0	0	1	0	1	0	1	$V_{L2}+V_{R2}-V_{R1}$
7	0	1	1	0	0	1	1	0	1	0	0	1	0	1	$V_{L2}+V_{R2}+V_H-V_{L1}-V_{R1}$
8	0	1	1	0	0	1	1	0	0	1	0	1	0	1	$V_{L2}+V_{R2}-V_{L1}-V_{R1}$
9	1	0	0	1	1	0	1	0	1	0	0	1	0	1	$V_{L1}+V_{R2}+V_H$
10	1	0	0	1	1	0	1	0	0	1	0	1	0	1	$V_{L1}+V_{R2}$
11	0	1	0	1	1	0	1	0	1	0	0	1	0	1	$V_{R2}+V_H$
12	0	1	0	1	1	0	1	0	0	1	0	1	0	1	V_{R2}
13	1	0	0	1	0	1	1	0	1	0	0	1	0	1	$V_{R2}+V_H-V_{L1}$
14	1	0	0	1	0	1	1	0	0	1	0	1	0	1	$V_{R2}-V_{L1}$
15	0	1	0	1	0	1	1	0	1	0	0	1	0	1	$V_{R2}+V_H-V_{R1}$
16	0	1	0	1	0	1	1	0	0	1	0	1	0	1	$V_{R2}-V_{R1}$
17	1	0	1	0	1	0	0	1	1	0	0	1	0	1	$V_{L2}+V_{R1}+V_H$
18	1	0	1	0	1	0	0	1	0	1	0	1	0	1	$V_{L2}+V_{R1}$
19	0	1	1	0	1	0	0	1	1	0	0	1	0	1	$V_{L2}+V_{R1}+V_H-V_{L1}$
20	0	1	1	0	1	0	0	1	0	1	0	1	0	1	$V_{L2}+V_{R1}-V_{L1}$
21	1	0	1	0	0	1	0	1	1	0	0	1	0	1	$V_{L2}+V_H$
22	1	0	1	0	0	1	0	1	0	1	0	1	0	1	V_{L2}
S NO	S_{L1}	S_{L2}	S_{L3}	S_{L4}	S_{R1}	S_{R2}	S_{R3}	S_{R4}	S_{H1}	S_{H2}	S_{H3}	S_{H4}	S_a	S_b	Vo
23	0	1	1	0	0	1	0	1	1	0	0	1	0	1	$V_{L2}+V_H-V_{L1}$
24	0	1	1	0	0	1	0	1	0	1	0	1	0	1	$V_{L2}-V_{L1}$
25	1	0	0	1	1	0	0	1	1	0	0	1	0	1	$V_{L1}+V_{R1}+V_H$
26	1	0	0	1	1	0	0	1	0	1	0	1	0	1	$V_{L1}+V_{R1}$
27	0	1	0	1	1	0	0	1	1	0	0	1	0	1	$V_{R1}+V_H$
28	0	1	0	1	1	0	0	1	0	1	0	1	0	1	V_{R1}
29	1	0	0	1	0	1	0	1	1	0	0	1	0	1	$V_{L1}+V_H$
30	1	0	0	1	0	1	0	1	0	1	0	1	0	1	V_{L1}
31	0	1	0	1	0	1	0	1	1	0	0	1	0	1	V_H
32	0 1	1 0	0 1	1 0	0 1	1 0	0 1	1 0	0 1	1 0	0 1	1 0	0 1	1 0	0
33	1	0	1	0	1	0	1	0	0	1	1	0	1	0	$-V_H$
34	0	1	1	0	1	0	1	0	1	0	1	0	1	0	$-V_{L1}$
35	0	1	1	0	1	0	1	0	0	1	1	0	1	0	$-(V_{L1}+V_H)$
36	1	0	1	0	0	1	1	0	1	0	1	0	1	0	$-V_{R1}$
37	1	0	1	0	0	1	1	0	0	1	1	0	1	0	$-(V_{R1}+V_H)$
38	0	1	1	0	0	1	1	0	1	0	1	0	1	0	$-(V_{L1}+V_{R1})$
39	0	1	1	0	0	1	1	0	0	1	1	0	1	0	$-(V_{L1}+V_{R1}+V_H)$
40	1	0	0	1	1	0	1	0	1	0	1	0	1	0	$-(V_{L2}-V_{L1})$
41	1	0	0	1	1	0	1	0	0	1	1	0	1	0	$-(V_{L2}+V_H-V_{L1})$
42	0	1	0	1	1	0	1	0	1	0	1	0	1	0	$-V_{L2}$

43	0	1	0	1	1	0	1	0	0	1	1	0	1	0	$-(V_{L2}+V_H)$
44	1	0	0	1	0	1	1	0	1	0	1	0	1	0	$-(V_{L2}+V_{R1}-V_{L1})$
45	1	0	0	1	0	1	1	0	0	1	1	0	1	0	$-(V_{L2}+V_{R1}+V_H-V_{L1})$
46	0	1	0	1	0	1	1	0	1	0	1	0	1	0	$-(V_{L2}+V_{R1})$
47	0	1	0	1	0	1	1	0	0	1	1	0	1	0	$-(V_{L2}+V_{R1}+V_H)$
48	1	0	1	0	1	0	0	1	1	0	1	0	1	0	$-(V_{R2}-V_{R1})$
49	1	0	1	0	1	0	0	1	0	1	1	0	1	0	$-(V_{R2}+V_H-V_{R1})$
50	0	1	1	0	1	0	0	1	1	0	1	0	1	0	$-(V_{R2}-V_{L1})$
51	0	1	1	0	1	0	0	1	0	1	1	0	1	0	$-(V_{R2}+V_H-V_{L1})$
52	1	0	1	0	0	1	0	1	1	0	1	0	1	0	$-V_{R2}$
53	1	0	1	0	0	1	0	1	0	1	1	0	1	0	$-(V_{R2}+V_H)$
54	0	1	1	0	0	1	0	1	1	0	1	0	1	0	$-(V_{L1}+V_{R2})$
55	0	1	1	0	0	1	0	1	0	1	1	0	1	0	$-(V_{L1}+V_{R2}+V_H)$
56	1	0	0	1	1	0	0	1	1	0	1	0	1	0	$-(V_{L2}+V_{R2}-V_{L1}-V_{R1})$
57	1	0	0	1	1	0	0	1	0	1	1	0	1	0	$-(V_{L2}+V_{R2}+V_H-V_{L1}-V_{R1})$
58	0	1	0	1	1	0	0	1	1	0	1	0	1	0	$-(V_{L2}+V_{R2}-V_{R1})$
59	0	1	0	1	1	0	0	1	0	1	1	0	1	0	$-(V_{L2}+V_{R2}+V_H-V_{R1})$
60	1	0	0	1	0	1	0	1	1	0	1	0	1	0	$-(V_{L2}+V_{R2}-V_{L1})$
61	1	0	0	1	0	1	0	1	0	1	1	0	1	0	$-(V_{L2}+V_{R2}+V_H-V_{L1})$
62	0	1	0	1	0	1	0	1	1	0	1	0	1	0	$-(V_{L2}+V_{R2})$
63	0	1	0	1	0	1	0	1	0	1	1	0	1	0	$-(V_{L2}+V_{R2})$

4. Simulation Model

Fig. 2 shows the simulation model of the proposed cascaded MLI. The switching pulse has been developed with the help of table 1 with the nearest control algorithm.

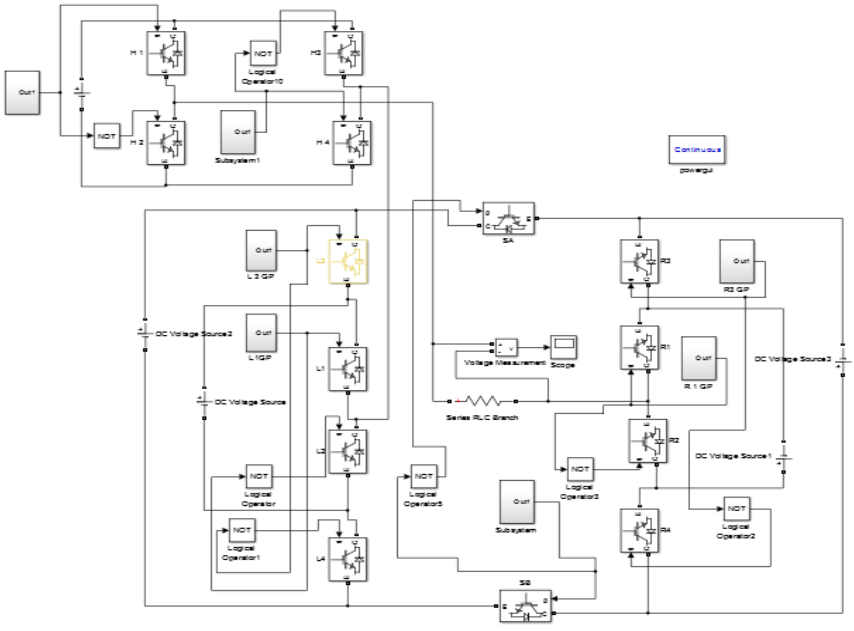

Fig.2. Simulation Model of the proposed cascaded MLI

5. Simulation Result

The simulation is done using **MATLAB** version **R2013a**. The switching pattern has been developed with the help of switching table 1. The switching pattern for all the power switches in the NDHB ($S_{L,1}$, $S_{L,2}$,$S_{L,3}$,$S_{L,4}$,$S_{R,1}$, $S_{R,2}$, $S_{R,3}$, $S_{R,4}$,S_a, and S_b) hasbeen developed for complete two cycles of reference time given in the Fig. from 3 to 12.

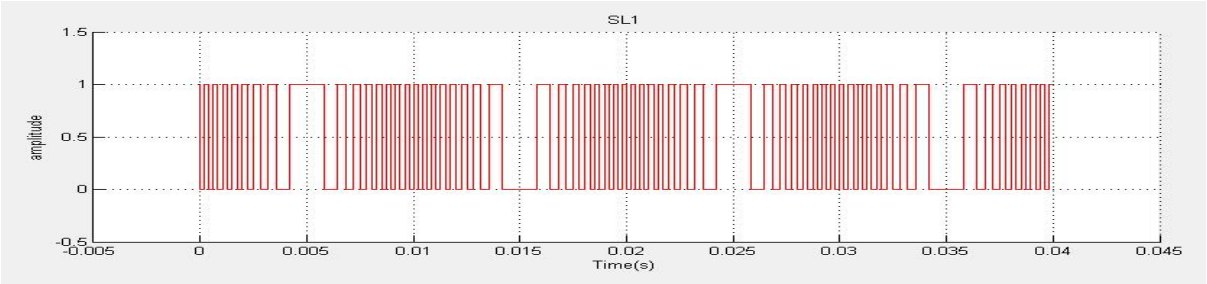

Fig.3. $S_{L,1}$ switching pattern

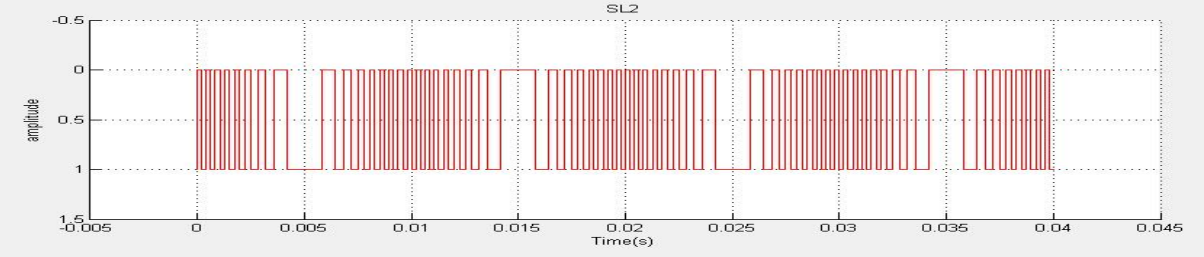

Fig. 4 $S_{L,2}$ switching pattern

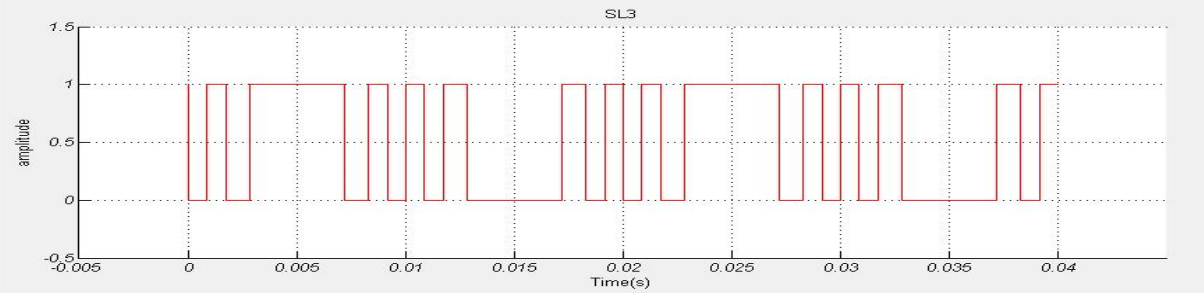

Fig. 5 $S_{L,3}$ switching pattern

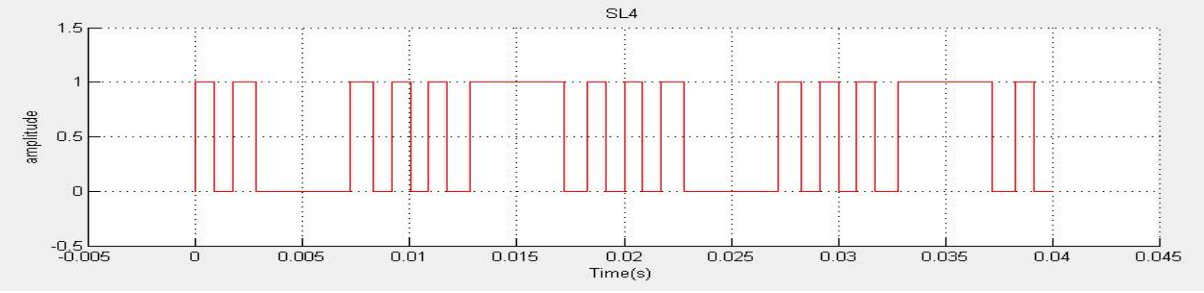

Fig. 6 $S_{L,4}$ switching pattern

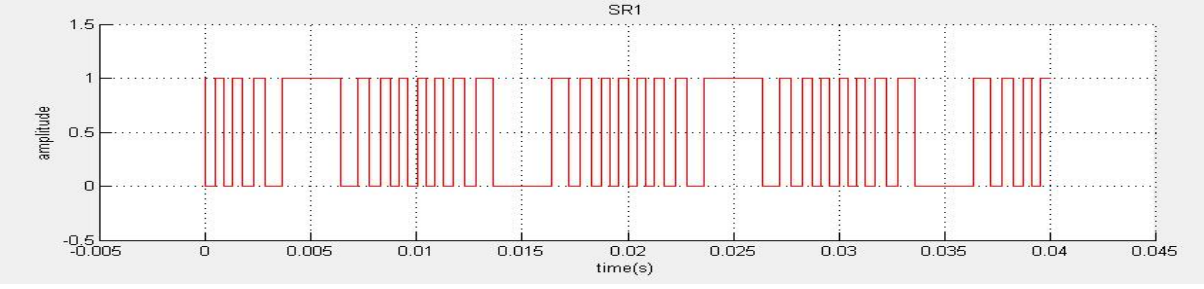

Fig. 7 $S_{R,1}$ switching pattern

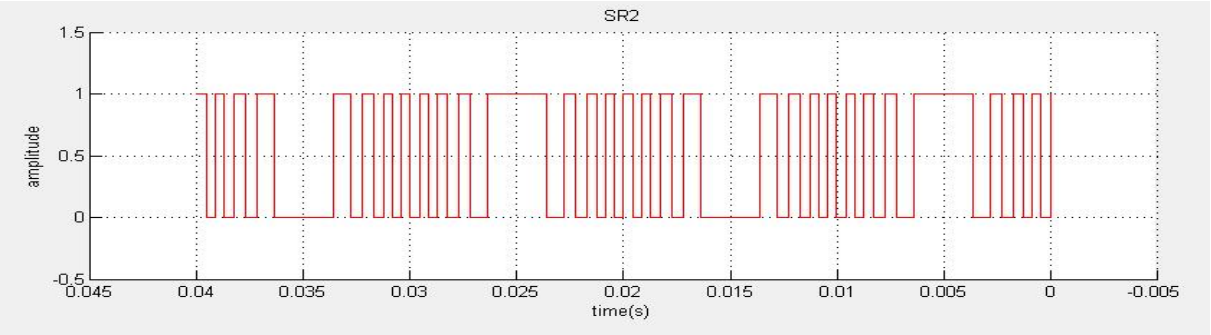

Fig. 8 $S_{R,2}$ switching pattern

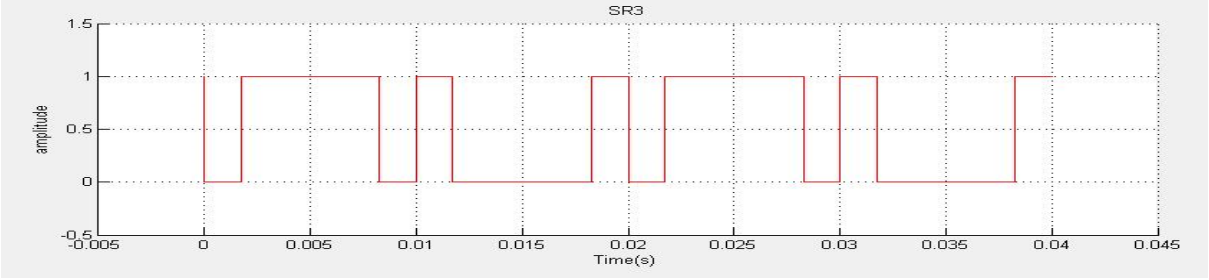

Fig. 9 $S_{R,3}$ switching pattern

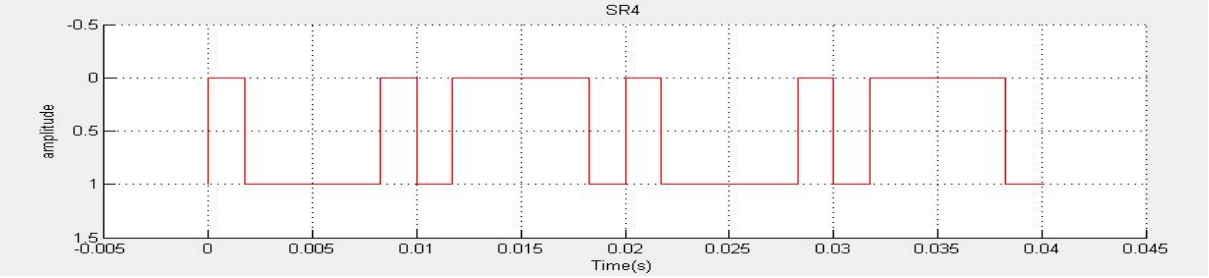

Fig. 10 $S_{R,4}$ switching pattern

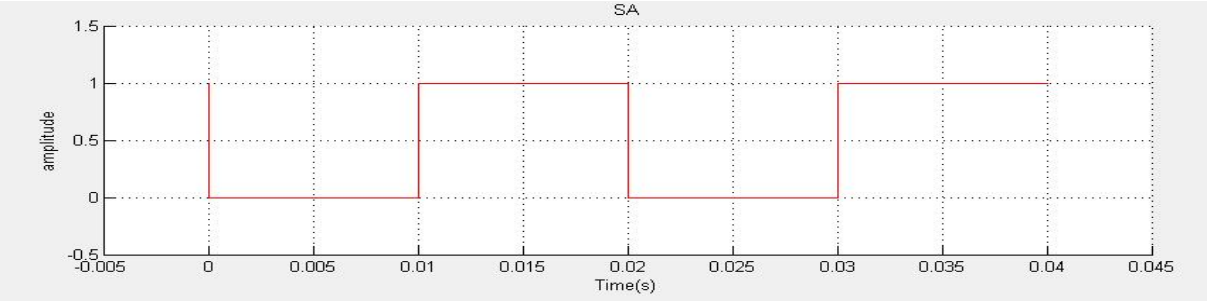

Fig. 11 S_a switching pattern

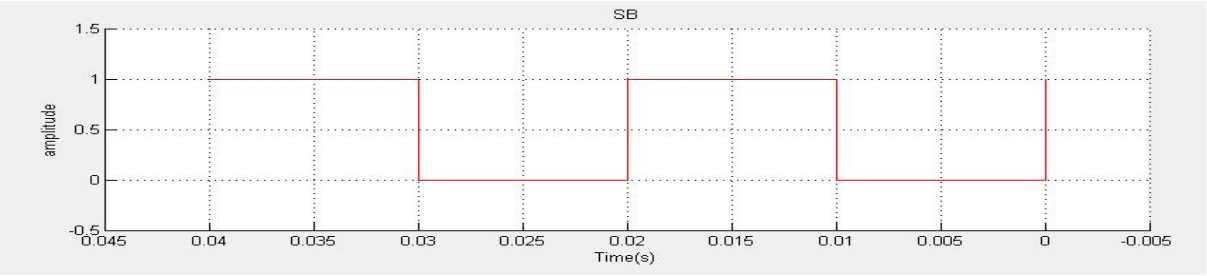

Fig. 12 S_b switching pattern

MATLAB Simulation results of the NDHB-MLI and overall cascaded MLI of thirty-one level and sixty-three level cascaded MLI is shown in Fig. 13 and 14 respectively.

Fig. 13 Thirty-one level output voltage of NDHB

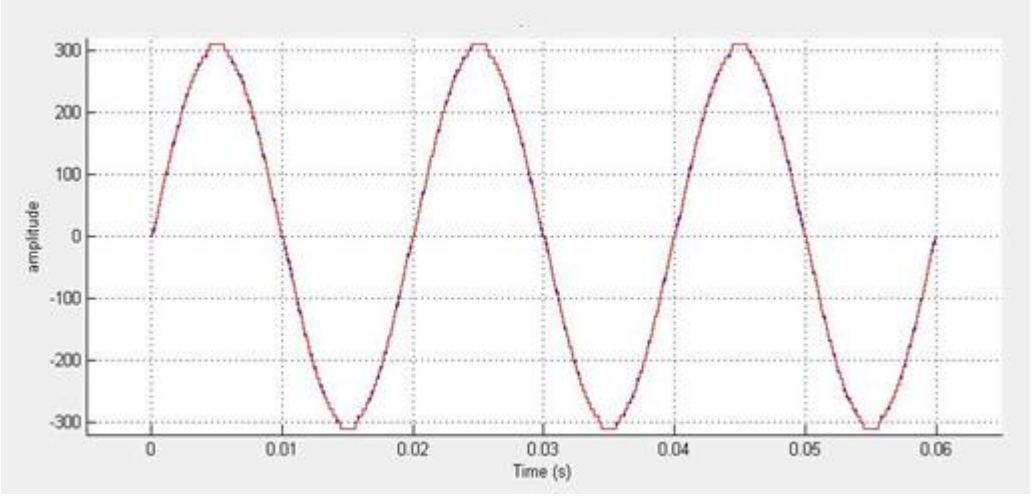

Fig. 14 Sixty-three level output Voltage of overall cascaded MLI

The FFT analysis of overall cascaded MLI sixty-three level cascaded MLI is shown in Fig. 15.

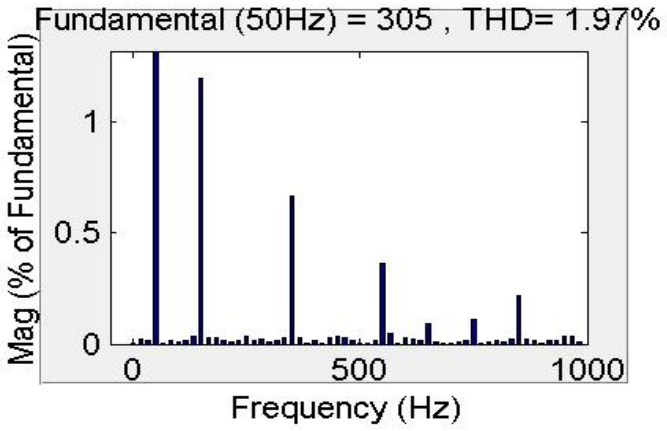

Fig. 15 FFT analysis of overall cascaded MLI

6. Conclusion

This paper presented a novel configuration of Single phase MLI, which is based on the cascaded connection of two different topologies.To generate both positive and negative voltage levels at the output, the nearest level control method is proposed to generate all possible combinations of voltage levels at the output. Based on this method, NDHB cascaded with HB, requires a lower number of power electronic switches, driver circuits, DC sources and less number of switches are in active conduction mode irrespective of the number of levels and DC sources in the MLI compared to Modified HB and cascaded HB based MLI. The proposed inverter can also reduce the THD at its output. Finally, the obtained simulation results of sixty-three levels verify the performance of the proposed MLI.

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