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Multiple Bit Adders with Re-Resourcing of Mux Adders

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A B S T R A C T

Adders are the basic elements used in complex data processing for efficient VLSI design. The CSLA adder circuit is used for the design of high speed processors. There is scope for decreasing the power and area of the design while preserving the speed of the circuit in CMOS technology. The CSLA adder architecture is such that it is of less power dissipation, area efficient and high speed. In this paper 4transistor XNOR gate is used to design the hybrid CMOS Full Adder circuit. The CSLA circuit is designed using this hybrid CMOS Full Adder circuit for 8-, 16-, 32-bit and parameters like area, power and delay are compared with that of the regular CSLA. Here the excess logic operations in the regular CSLA are eradicated and a new logic operation for the modified CSLA is formulated before the final sum calculation is proposed. The power consumed by the modified XNOR and Full adder is 0.5595mW and 1.273mW respectively. In this paper design work is compared with the regular CSLA adder with parameters like area, power and delay through 180nm CMOS process technology and implemented in Cadence Virtuoso tool. The results show that modified CSLA is more efficient than the conventional CSLA in terms of area, power and delay.

Keywords: CMOS, Adder, Mux Adder, pMos, nMos

1. Introduction

The low power - area efficient and high speed logic data path system design is the interesting areas of research in VLSI. In any processor adders are the main components of the ALU which defines the speed of any processor. A digital circuit that accomplishes digital addition is called as an adder. In numerous PCs and different kinds of processors, adders are utilized in arithmetic logic units or ALUs. They are additionally utilized in different pieces of the processor to ascertain addresses, table indexes, augmentation and decrement operators, and so forth.Adder is a basic and indispensable circuit for arithmetic operations in digital system. Careful design and analysis of adder is most important for the speedy and accurate function of overall electronic system. Ripple Carry Adder is used for executing addition operation for N-bit numbers. It is designed by cascading N number of full adder for adding two N-bit number. Comparing with other adders, Ripple Carry Adder is simple to design but consumes more delay since the carry bit of last full adder is valid only after the joint propagation delay of all full adder cascaded.

As technology scaling continued, allowing for more logic gates per chip, complex parallel prefix schemes with different algorithms, yielding fast adder designs along with improvement in power and energy consumption became viable. Two such addition algorithms are Weinberger's recurrence and ling's recurrence which are based on parallel computation of carry to increase the addition speed by reducing the delay. These two adders also provide techniques to reduce the energy consumption. Manchester carry chain adder having cascaded architecture provides efficiency in area.In spite of the fact that it is conceivable to build adders for some advanced portrayals, for example, parallel coded decimal or more than 3, the most widely recognized adder works on twofold 6 numbers. On account of utilizing two supplements or one supplement to speak to a negative number, the adder is adjusted to an adder - the subtractor is inconsequential. Other marked numbers demonstrate more logic around the essential adder.

Recent progress in CMOS (Complementary Metal Oxide Silicon) integrated circuits (ICs) and SiGe HBT technologies has made it possible to consider silicon technology as an alternative means for realization of capable and economical systems that operate at 200 GHz and higher. This dissertation discusses the devices available in CMOS, and fundamental circuit building blocks of sub-millimeter wave systems (signal sources, detectors and antennas) operating between 100 and 700 GHz fabricated using the devices. Based on these, this dissertation suggests paths for achieving terahertz CMOS circuits and systems as well as the challenges.

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2. Literature Survey

The architecture is based on a chain of full-adder cells (FA), Figure 1. We refer to this adder as RCA. The complexity and the time delay is linear with the number of bits. It is considered the standard and the easier architecture that can be designed, in terms of area complexity, but also the slower one, in terms of propagation delay. The critical path is the carry chain, where each FA must wait the delay of the previous cout stage. Equation below gives the expected propagation delay of a 16-bit RCA, where tFAc is the worst FA's path delay generating cout (a to cout for the first FA and cin to cout for others). [1]

$$t_p \approx 16t_{FA_c}$$

Because of the importance of floating point arithmetic in different field of computation many different approaches and structures have been already presented, this section presents a short review of some of them found useful for the proposed work. Michael L. Overton [2] written a great literature on the details of floating-point presentation of different IEEE standards with examples for understanding of such systems. Different types of adders (Carry Adder, Ripple Carry Adder, etc.) with different approaches (Parallel Adders, High-speed Adders, and Low-power High-performance Adders) have been presented in [3][4]. Pongyupinpanich Surapong et al [5] presented the CORDIC Algorithm based Floating-Point Division Operator, for that they developed an efficient architecture of CORDIC algorithm to make its processing capability much broader input ranges. The optimization algorithm for CORDIC-based FFT units with Fixed-Point Accuracy Analysis is presented by Omid Sarbishei et al [6]. The mathematical co-processor core for 32-bit floating-point capable of handling over flow, under flow and special number (infinity and not-anumber) representations, using the CORDIC algorithm is presented by Tanya Vladimirova et al [7]. The coprocessor also facilitates thirteen elementary functions (like adding, subtracting etc.). The non- CORDIC approach for floating point multiplier with technology independent pipelined design is presented by Mohamed Al-Ashrafy et al [8]. The multiplier implementation also handles the overflow and underflow cases. The performance analysis of different floating point multiplier designs are presented in [9]. Self-Timed Asynchronous Sub-threshold Logic systems are studied by Niklas Lotze et al [10], with discussion for necessary timing overheads and approach for their analysis and reduction by the use of circuit techniques. Implementation of Phased Logic (PL) systems by selftimed programmable architecture is discussed by Cherrice Traver et al [11].

Many researches have been proposed regarding the 1-bit multiplexer-based FA. Research [3] presents FA of six multiplexers with 12 transistor in total, which is a low power consumption design. The multiplexer of MBA-12T [3] adopted PTL logic which requires only two transistors. This is in order to reduce switching activities and short-circuit current. However, the drivability of MBA-12T is weak that cause poor performance and more sensitive. Because the MBA- 12T does not directly connect to the power-supply, this kind of the circuit relies on the buffers in each stage for drivability.

Full adder can be composed of three main blocks as shown Fig. 2 (a). This structure is the most of implementation of the 1-bit full adder [1]. The block1 generated AB and A B from XOR and XNOR operation. The block2 generated Sum by the results of block1 and Cin; the block3 generated Cout by results of block1 and inputs. This design can balance delay on the output of FA and can abated glitch in the circuit.

In [4], block2 and block3 are implemented by two multiplexers as shown in Fig. 2(b). The output of block2 is Sum and the output of block3 is Cout. Even so, this design is slightly different, A or B and AB are the inputs of multiplexer in block2, and AB and AB are the inputs of multiplexer in block3. These multiplexers are employed PTL, and other internal logic use double pass-transistor logic (DPL) or swing restored CPL (SR-CPL).

3. Proposed Work

There are two type of one-bit adders, Full Adder and one is half adder, the proposed algorithm here uses the full adder as it does not decline any carry bit and hence the outputs are much more accurate, precise and reliable too.

Using full bit adder to construct multiple bit adders can be useful as the single block of an adder can be used again and again to addmultiple bits, also it will be requiring less area and hence resulting in less power consumption.

Mux adders are more complex code blocks which allows the system to draw a lesser path and lesser time for the execution of the whole process. Multiplexer (MUX) select one input from the multiple inputs and forwarded to output line through selection line. It consists of 2 power n input and 1 output. The input data lines are controlled by n selection lines.

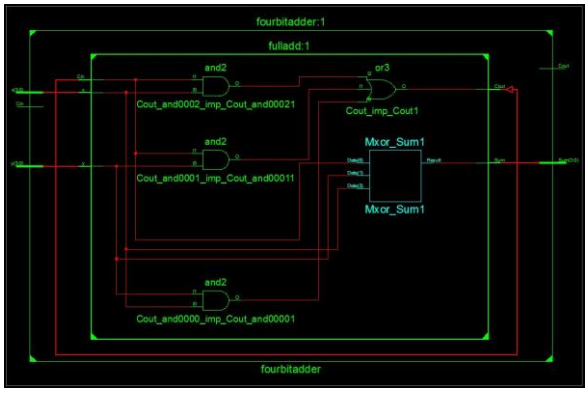

Figure 1. Four Bit Adder RTL Schematic by Xilinx

A Four-bit Ripple-Carry adder is an iterative combinational circuit. It consists of four full adder stages connected in cascade, each of which handles one bit. The carry output of each full adder is connected to the carry input of the next most significant full adder. The figure clearly shows that the carry bit ripples through a chain of the cascaded FAs, from a lower bit to the next higher order bit. A worst-case addition will require the carry to ripple from the position of the least significant bit to that of the most significant bit. The worst-case delay increases linearly with the length of the carry propagation path, which depends on the number of the bits processed by the operands.

Four-bit adder constructed here is designed and developed over the bus input module and bus output module.The designed module is successfully synthesized in Xilinx but maps ported by the RTL schematic could be better, another four-bit adder has been designed to overcome the RTL schematic MAP issue as shown in figure 2.

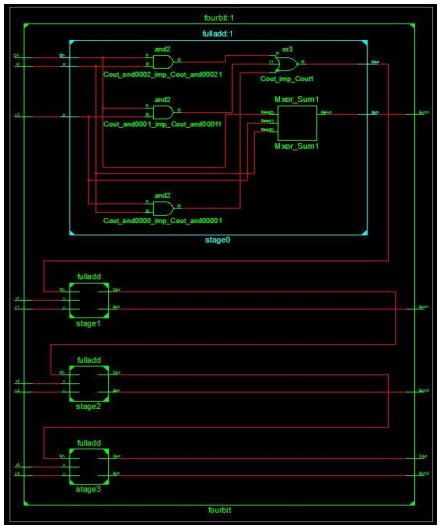

Figure 2: Four Bit adder with individual Full Adder Module

8-bit adder module can be designed by extending the above designed 4-bit adder. The designed RTL Schematic though can be modified by using the minimum block set of the full adder, it can be designed using the mux and four bit adder as well.

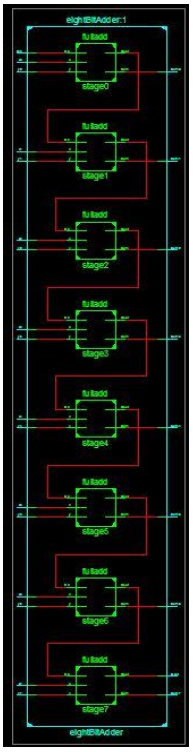

Figure 3: Eight bit Adder RTL Schematic

4. Result

The designed 32- bit adder has been successfully synthesized and implemented over the FPGA device by Xilinx Spartan3 XC3S1500L.

Table 1: Comparison of 32-bit adder Designs

Design	LUTs	Slices	Delay(ns)	Fan-out
RCA[]	64	37	38.665	1.74
C1NA[]	88	50	26.57	2.15
CBYA[]	101	56	25.514	2.53
Our Design	64	48 (37 Estimated)	24.097	1.74

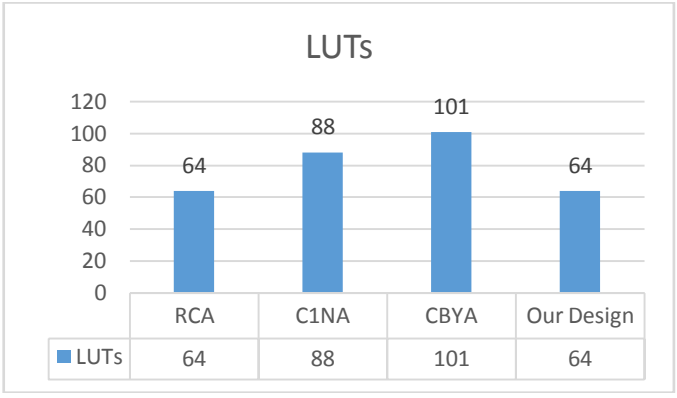

Figure 4: LUT Comparison Graph

5. Conclusion

Carry select adders are frequently used for the high speed arithmetic operations. The carry select adder is composed of two 4-bit ripple carry adders in each section both carry and sum bits are calculated for the two input carry Cin=0 and Cin=1. Further for 16bit three such ripple carry blocks with one four bit RCA block as first section. Each section's carry out will be the carry in for the next section which will select the appropriate RCA for final out. The section will grows similarly for higher bit CSLA design. Many research authors have been done successful work in regarding the optimization of area and power efficient FA and carry select adder with CMOS full adder block sections inside the ripple carry adder blocks. RCA blocks are the cascaded for of the full adders.

The proposed work is having slight increase in the area but is of time efficient adder circuit with full test bench and FPGA swing at the output. The adder can be further implemented for 64-, 128- bit Adder by using the optimization method to reduce the power area and delay of the circuit.

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