WWW.IJRPR.COM

International Journal of Research Publication and Reviews

Journal homepage: www.ijrpr.com ISSN 2582-7421

High-Speed and Low-Power Multipliers Using Modified HPM-Based Baugh-Wooley Multipliers Algorithm

T.Kannan[1], S.Vinoth Kumar[2], R.Prabu[3]

Assistant Professor, ECE, Paavai College of Engineering, Namakkal, India[1]

Assistant Professor, ECE, Paavai College of Engineering, Namakkal, India[2]

Assistant Professor, ECE, Paavai College of Engineering, Namakkal, India[3]

A B S T R A C T

Multiplier is a heavily used mathematical process in digital signal processing and scientific applications. With approaching technologies, several researchers have tried and area unit hard to style high performance, low power consumption, little space implementation. This paper proposes a high speed multiplier style victimization VHDL (Very High Speed Integrated Circuits Hardware Description Language). The Baugh- Wooley formula is acting unsigned multiplication and two's complement. In changed Baugh- Wooley the important path delay has been reduced by victimization M-HPM tree conception and also the speed is increased. It's used ordinarily because the quickest number. Baugh Wooley number is another technique for signed multiplicati on. it's not wide used attributable to its quality of its structure. Here the look of 8-bit changed Baugh- Wooley number has been designed and enforced by standard technique and conjointly victimization High- Performance number Reduction tree (HPM) technique. The comparative analysis of all the look for the delay, space foot print and energy has done victimization Xilinx ISE 13.2 to indicate that Baugh Wooley number will become a lot of quicker. The results area unit evaluated and synthesized using Xilinx has been chosen for simulation.

Keywords:Multiplier, Baugh Wooley, M-HPM and XilinxTool.

1. Introduction

Multiplication could be a advanced operation, that is mirrored in its comparatively high signal propagation delay, high power dissipation, and huge space demand. once selecting a multiplier factor for a digital system, the bit dimension of the multiplier factor is needed to be a minimum of as wide because the largest quantity of the applications that square measure to be dead on it digital system. The bit dimension of the multiplier factor is, therefore, typically a lot of larger than the info drawn within the operands, that ends up in unnecessarily high power dissipation and excess long delay [1][3].The most a part of this paper is that the reduction tree technique that is employed for coming up with a brand new Baugh Wooley multiplier factor design.

High Performance multiplier factor (HPM) reduction tree relies primarily on the generated partial product compression. It's fully regular and therefore the property of the adding cells in HPM is within the triangular form. The rationale for victimization triangular formed is that the triangular cell placement within the reduction tree technique incorporates a shorter wire length.In the paper style and implementation of standard eight bit unsigned Baugh Wooley and High Performance multiplier factor rule has done and compared the result obtained with the new style of eight bit unsigned Baugh Wooley and biological warfare multiplier factor rule victimization HPM reduction tree. The

comparative analysis has been done to prove that the new Baugh Wooley multiplier factor styleis quicker than the traditionalBaugh Wooley. The rule for four bitunsigned Baugh Wooley multiplierfactor is shown in Fig 1.

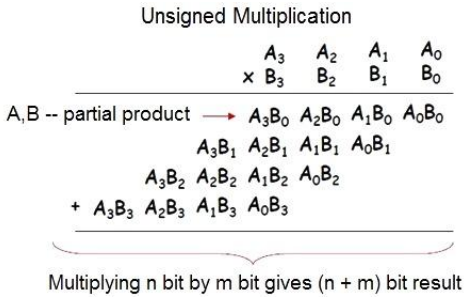


Fig-1: Illustration of 4 bit unsigned Multiplier Algorithm.

2. TWIN-PRECISION FUNDAMENTALS

Initially we have a tendency to gift the twin-precision technique exploitation associate degree illustration of unsigned binary multiplication. In associate degree unsigned binary multiplication every little bit of one amongst the operands, referred to as the multiplier factor, is increased with the second quantity, referred to as number [1].

$$P_{ij} = X_i Y_j$$

						x_7	x_6	x_5	x_4	x_3	x_2	x_1	x_0
						y_7	y_6	y_5	y_4	y_3	y_2	y_1	y_0
					0	p_{70}	p_{60}	p_{50}	p_{40}	p_{30}	p_{20}	p_{10}	p_{00}
				p_{71}	p_{61}	p_{51}	p_{41}	p_{31}	p_{21}	p_{11}	p_{01}		
			p_{72}	p_{62}	p_{52}	p_{42}	p_{32}	p_{22}	p_{12}	p_{02}			
		p_{73}	p_{63}	p_{53}	p_{43}	p_{33}	p_{23}	p_{13}	p_{03}				
	p_{74}	p_{64}	p_{54}	p_{44}	p_{34}	p_{24}	p_{14}	p_{04}					
p_{75}	p_{65}	p_{55}	p_{45}	p_{35}	p_{25}	p_{15}	p_{05}						
p_{76}	p_{66}	p_{56}	p_{46}	p_{36}	p_{26}	p_{16}	p_{06}						
p_{77}	p_{67}	p_{57}	p_{47}	p_{37}	p_{27}	p_{17}	p_{07}						
s_{15}	s_{14}	s_{13}	s_{12}	s_{11}	s_{10}	s_9	s_8	s_7	s_6	s_5	s_4	s_3	s_2	s_1	s_0

Fig-2: Diagram of 8 bit unsigned Multiplier Algorithm

In that method one row of partial product is generated. Every row of partial product is shifted in step with the position of the little bit of the multiplier factor, forming what's unremarkably referred to as the partial-product array. Finally, partial product that ar within the same column ar summed along, forming the ultimate result. associate degree illustration of associate degree 8-bit multiplication is shown in Fig. 2.

3. BAUGH WOOLEY MULTIPLIER

The Baugh-Wooley multiplication is one amongst the economical ways to handle the sign bots. This approach has been developed so as to style regular multipliers, suited to 2's complement numbers. Let 2 n-bit numbers, multiplier factor (A) and number (B), to be increased. A and B are often delineated as

$$A = -a_{n-1}2^{n-1} + \sum_{i=0}^{n-2} a_i 2^i$$

$$B = -b_{n-1}2^{n-1} + \sum_{i=0}^{n-2} b_i 2^i$$

Where the a_i's and b_i's are the bits in A and B, respectively, and a_{n-1} and b_{n-1} are the sign bits[2][6]. The product, P = A x B is given by the equation:

a. Algorithms for Baugh–Wooley

The BW algorithm formula may be a relative easy method of playacting signed multiplications. Fig. three illustrates the formula for associate degree 8-bit case, wherever the partial-product array has been reorganised in step with the theme of Hatamian [1]. The creation of the reorganised partial-product array contains 3 steps: i) the foremost vital partial product of the primary N - one rows and therefore the last row of partial product except the foremost vital got to be negated, ii) a relentless one is intercalary to the ordinal column, iii) the foremost vital bit (MSB) of the ultimate result's negated[1].

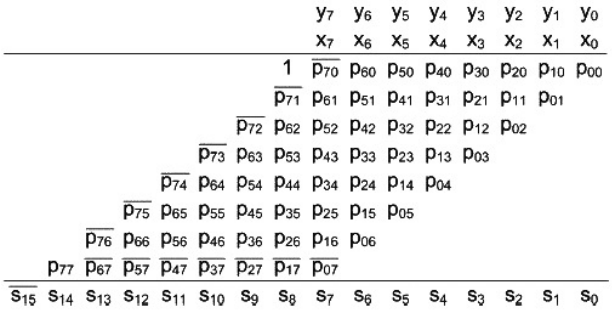


Fig-3: Diagram of a signed 8-bit multiplication, using the Baugh–Wooley algorithm.

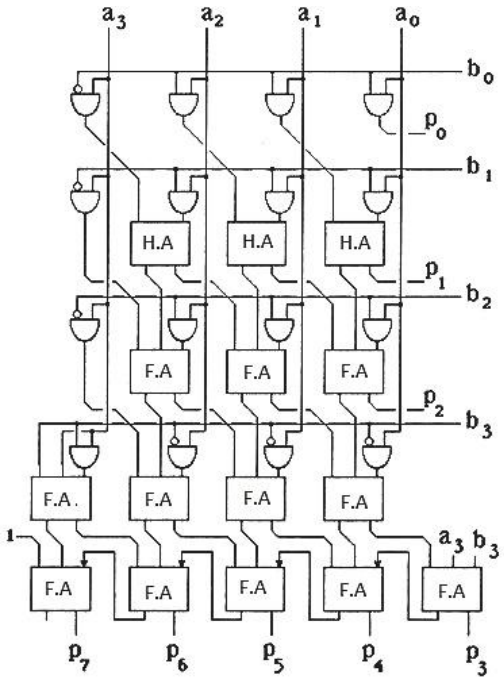


Fig-4: Block diagram of a signed 8-bit multiplication, using the Baugh–Wooley Architecture.

4. HIGH PERFORMANCE MULTIPLIER TREE

In High Performance reduction tree technique the first partial product bits are generated outside the tree. Once the generation of partial product bits; these partial product then place into the reduction tree to calculate the merchandise of the number [2]. this may be done mistreatment range of half adders and full adders planned during a tree structure.

a. M - HPM Baugh Wooley Multiplier

The conventional Baugh Wooley number may be altered and created it as high performance Baugh-Wooley number by calculative the partial product mistreatment AND gates, array of half adders and arrangement the complete adders during a tree structure as shown within the fig.6. The tree structure arrangement can minimize the routing wire length and thus performance are increased [2] [6]

Implementation of eight bit unsigned Baugh Wooley number mistreatment M - HPM methodology is just a straightforward methodology that is as drawn within the rule. The partial product may be calculated exploitation AND gates, half adder and full adder. These partial product may be calculated using CLA. Insertion of zero and therefore the partial product ar shown in Fig.6.That the design of eight bit unsigned Baugh Wooley number mistreatment HPM [6].

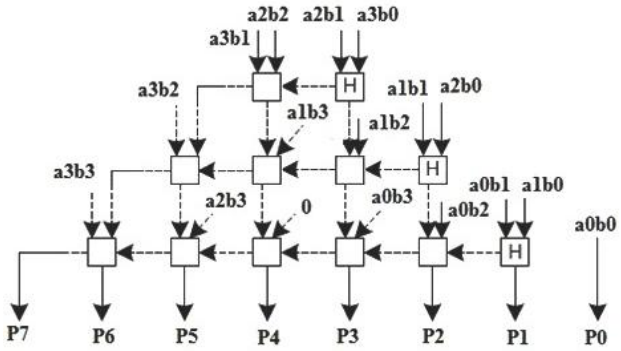


Fig-5: High Performance architecture for 4 bit unsigned Baugh Wooley multiplier.

For highspeed and/or low-power implementations, a reduction tree with exponent logic depth, like TDM, Dadda, Wallace or HPM [1] is most well-liked for summation of the partial product. Such a log-depth reduction tree has the advantage of shorter logic depth[9].

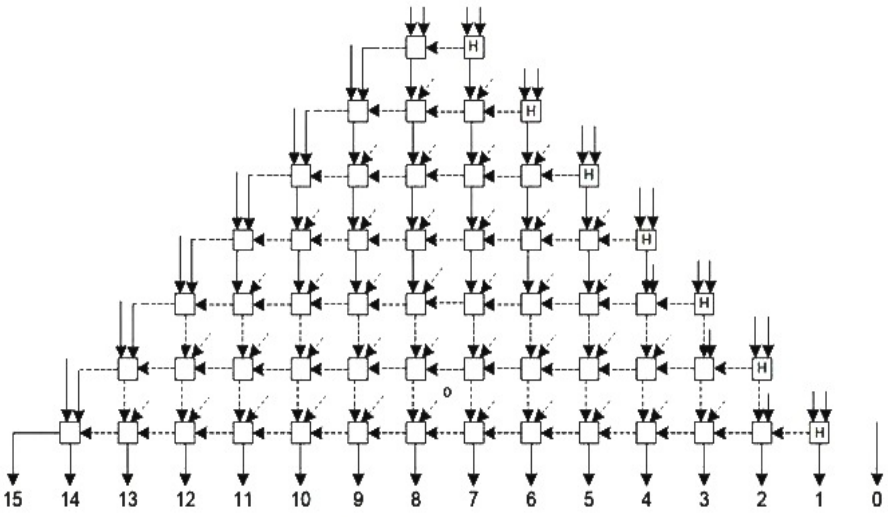


Fig-6: M - High Performance Architecture for 8 bit unsigned Baugh Wooley multiplier.

5 SIMULATION RESULTS

In this study, Simulation of 8 bit unsigned M - HPM Baugh Wooley Multiplier is implemented in VHDL and logic simulation is done by using ModelSim software and the synthesis is done using Xilinx ISE 13.2

Fig-7: Simulation results for 8-bit ModifiedHPM Tree based Baugh Wooley algorithm.

a. RTL Diagram

RTL is Register Transfer Level. It describes the route through which the data transfer take place. It captures the behaviour and converts it into circuit.

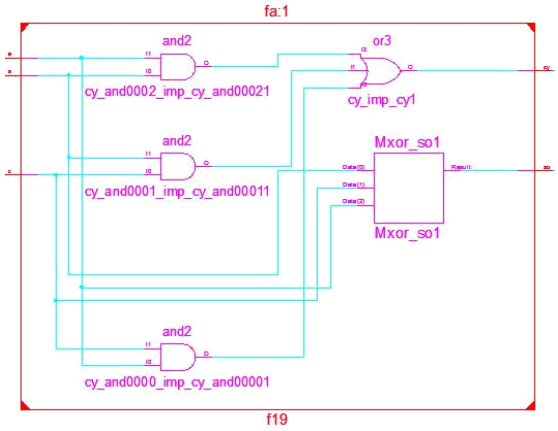


Fig-8: RTL View of Full adder

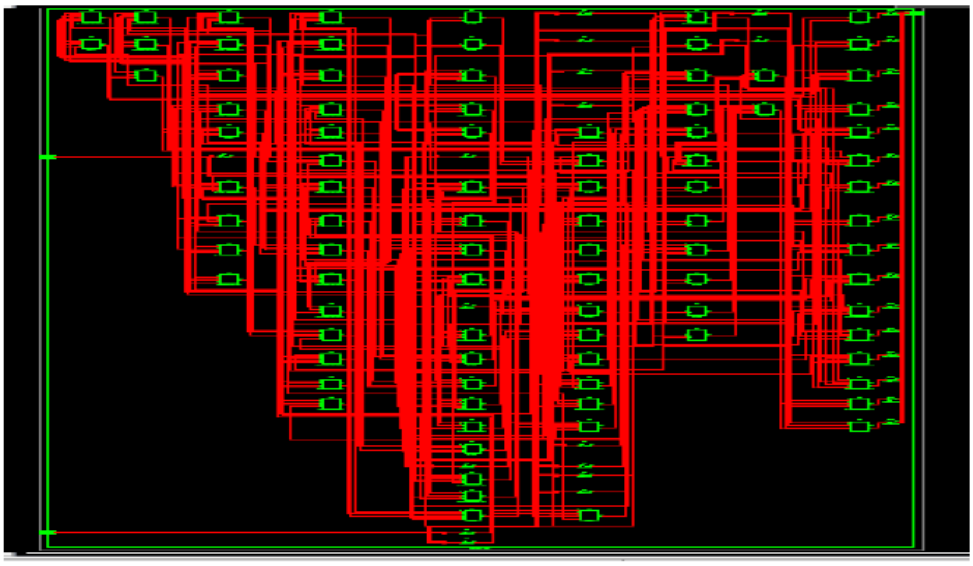


Fig-9: RTL View of 8-bit Conventional Baugh Wooley Multiplier.

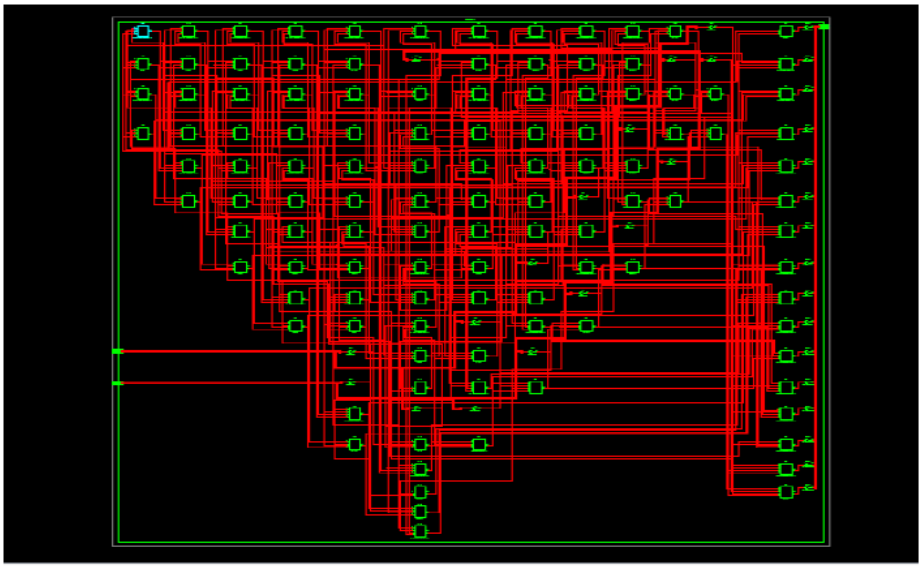
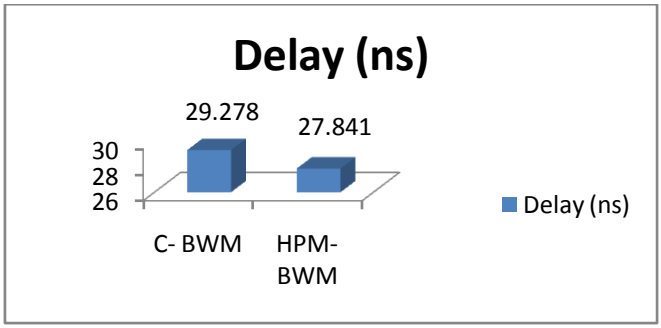


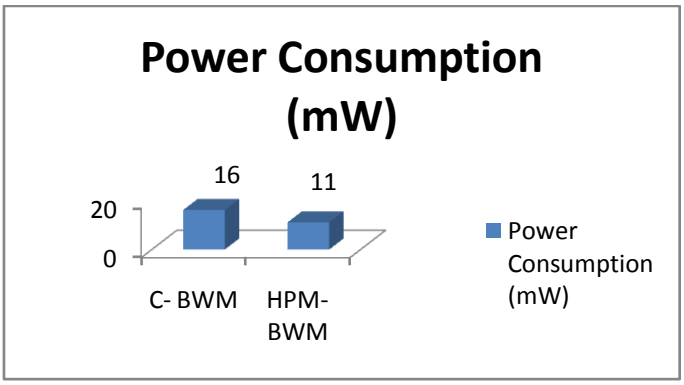
Fig-10: RTL View of 8-bitModified HPM Baugh Wooley Multiplier

6. COMPARISON CHART

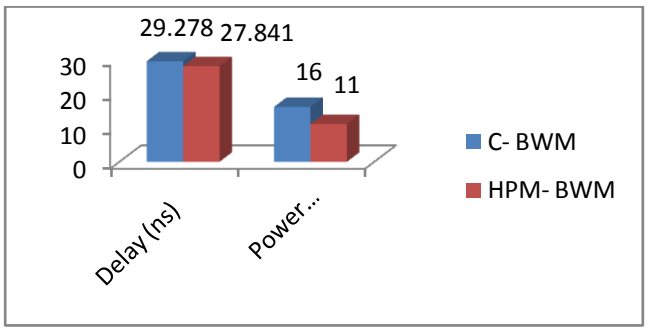
a. Comparison Chart of Multiplier for Delay:



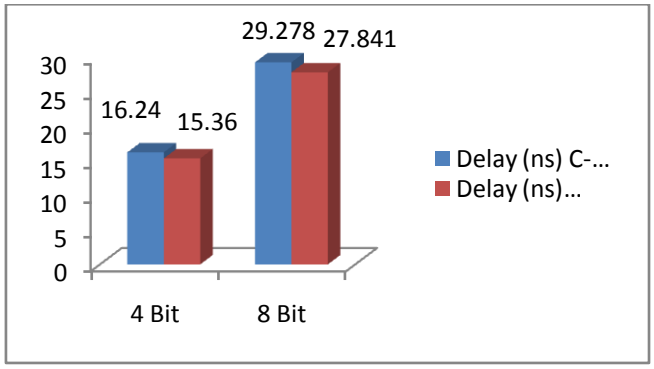
b. Comparison Chart of Multiplier for Power Consumption:



c. Comparison Chart of Multiplier for Delay and Power Consumption:



d. Comparison Chart of Multiplier for 4 bit and 8 bit Delay:



7. COMPARATIVE ANALYSIS

Analysis is done between the conventional Baugh Wooley Multiplier and Modified HPM Baugh Wooley Multiplier.

Table-1: Observations of Delay (4 bit & 8 bit) for Conventional Baugh Wooleymultiplier and M-HPM Tree based Baugh Wooley multiplier.

Parameter	**Conventional Baugh Wooley**		**M - HPM Baugh Wooley**	
Delay(ns)	4 bit	8 bit	4 bit	8 bit
	16.24	29.27	15.36	27.84

This above table gives the analysis of both the multipliers. In this table-1 the conventional as well as modified multipliers is compared. By the analysis we have come to know that modified HPM Baugh Wooley is faster when compared to conventional.

Conventional Baugh Wooley Multiplier versus HPM Tree based Baugh Wooley Multiplier in terms of delay,

power, area footprint and No. of LUTs. It is shown in Table 2.

Table-2: Observations of Conventional Baugh Wooleymultiplier and HPM Tree based Baugh Wooley multiplier.

Parameter	HPM Baugh Wooley	Conventional Baugh Wooley
Delay	27.841ns	29.278ns
Power Consumption	11mW	16mW
Area foot-print	15.511ns route (55.7% route)	16.469ns route (56.2% route)
No. of LUTs	114	121

8. CONCLUSION

Analysis of changed HPM Baugh-Wooley number and standard strategies has been designed and enforced still as synthesized in Xilinx ISE 13.2 simulation. The simulation result and RTL schematic of the modified HPM Baugh-Wooley and standard number is shown in Figure 8.2. The Baugh-Wooley multiplier of the delay time is calculated for **4bit** is **16.247ns** and for **8 bit** is **29.27ns**.Then the Modified HPM Baugh-Wooley multiplier is calculated for **4 bit** is **15.36ns** and for **8 bit** is **27.84ns**. From the delay calculation it is found that, the Modified HPM Baugh - Wooley multiplier performs better.

REFERENCES

[1] Magnus Själander and Per Larsson-Edefors, Senior Member, IEEE "Multiplication Acceleration Through Twin Precision" IEEE Transactions On Very Large Scale Integration (Vlsi) Systems, vol. 17, no. 9, September 2009.

[2] Jipsa Antony, JyotirmoyPathak" Design And Implementation Of High Speed Baugh Wooley And Modified Booth Multiplier Using Cadence RTL" IJRET - Volume: 03 Issue: 08, Aug-2014.

[3] M. Själander and P. Larsson-Edefors, ―The Case for HPM-Based Baugh-Wooley Multipliers,‖ Department of Computer Science and Engineering, Chalmers University of Technology, Tech. Rep. 08-8, March 2008.

[4] PramodiniMohanty., ―An Efficient Baugh-Wooley Architecture for both Signed & Unsigned Multiplication‖ (IJCSET) Vol. 3 No. 4 April 2012.

[5] Magnus Själander and Per Larsson-Edefors "High-Speed and Low-Power Multipliers Using the Baugh-Wooley Algorithm and HPM Reduction Tree".

[6] VinodSajjan, B.SajidhaThabassum, Mala Sinnoor "Design and Implementation of 4-Bit Unsigned Array Multiplier and Baugh Wooley Multiplier using CMOS 180nm Technology and Their Comparative Analysis" (IJSETR) - ISSN 2319-8885 Vol.04, Issue.02 January-2015.

[7] Ramesh Kumar Mallavarapu, TotaSrinivasaRao, "Design and Implementation of an Eight Bit Multiplier Using Twin Precision Technique and Baugh-Wooley Algorithm" - IJSR Publications, Volume 3, Issue 4, April 2013, ISSN 2250-3153.

[8] R.ArunSekar, B.Gopinath, "High Performance Baugh Wooley Multiplier Using Carry Skip Adder Structure"- (IRJET) Volume: 03 Issue: 02, Feb-2016.

[9] Magnus Sj¨alander, Henrik Eriksson, and Per Larsson-Edefors**"**An Efficient Twin-Precision Multiplier"- IEEE International Conference on Computer Design (ICCD'04).