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Design and Implementation of FIR and IIR Filters

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ABSTRACT

We will propose a design and implementation of FIR and IIR filters for system on chip design in this work. Our research aims to analyze and construct a system on chip for two common types of digital filters: FIR and IIR. The suggested filter processor is implemented and verified using the VERILOG hardware description language (HDL).

Keywords: ASIC, Digital System Design, Digital Filters, and Verilog HDL

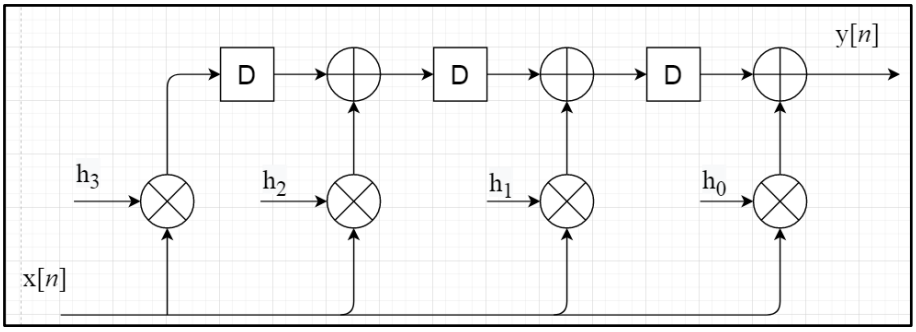
I. Introduction

The filters can be classified into analogue and digital filters based on how they classify input signals. An analogue filter is a device that incorporates multiple analogue components like as resistors, capacitors, and inductors and is used in a variety of applications such as noise reduction, video signal enhancement, and graphic equalization. A digital filter, on the other hand, works with discrete input signals. As a result, it performs a number of calculations on sampled signal values, as well as the overall system model of the digital filter [1]. In comparison to analogue filters, digital filters offer numerous benefits. Digital filters have the advantages of being programmable and simple to build, test, and implement. The digital filter, its design, and its use are the topic of this study.

Because a digital filter calculates discrete signals, the analogue input signal must be sampled and digitalized first [2]. As a result, in an overall digital system depicted in Figure 2, the digital filter is placed after the ADC, and the output of the digital filter is controlled to be input to the Fast Fourier Transform (FFT) [3] module or to be controlled to be input to the Digital-Analogue-Converter to convert back to a suitable analogue form. A digital filter is a crucial component of any digital system, whether it's a general-purpose computer or a specialized DSP chip. Our paper is organized as follows to clarify the proposed method: Sec. 2 describes the design and implementation, whereas Sec. 3 explains the conclusion.

II. Design and Implementation of FIR and IIR Filters

A moving average or smoothing filter is the simplest fundamental application of a FIR filter [4]. When $h_1 = h_2 = h_3 = h_4$ for example, we get an average module of order 4. In Figure 3, we use MATLAB to model order 4, 20 FIR filters. The input signal x is just a random number, and its graph is displayed in the first paragraph at the right corner. The FIR filters outputs for order-4 and order-20 are y4 and y20. Those paragraphs have been highlighted. As the figure shows, the higher the order number, the more smoothing output we obtain. One of the most common uses of the FIR filter is in the pressure part of a connection between an active pen and a touch screen, where the 8-bit input is expanded to 10-bits (1024 pressure levels) with the use of appropriate coefficients.



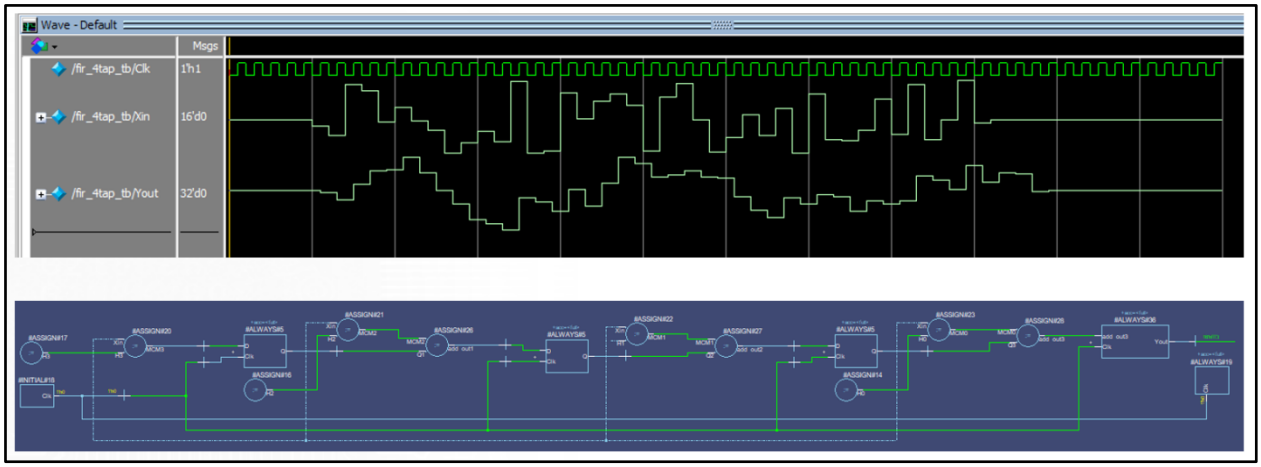


Figure 1: FIR Filter Design and Implementation

The infinite impulse response (IIR) receives its name because its impulse response recursively or feedback extends for an endless period.

$$\sum_{i=0}^{K} \alpha_i \times y[n-i] = \sum_{i=0}^{K} \beta_i \times x[n-i],$$

where x is input signal, y is filtered output, K is filter order, and α_i, β_i are coefficient of filters, $\alpha_0 = 1$. As the equation for IIR filter [5], the corresponding block diagram is explained as figure 2 where we can use several sessions in the filter design.

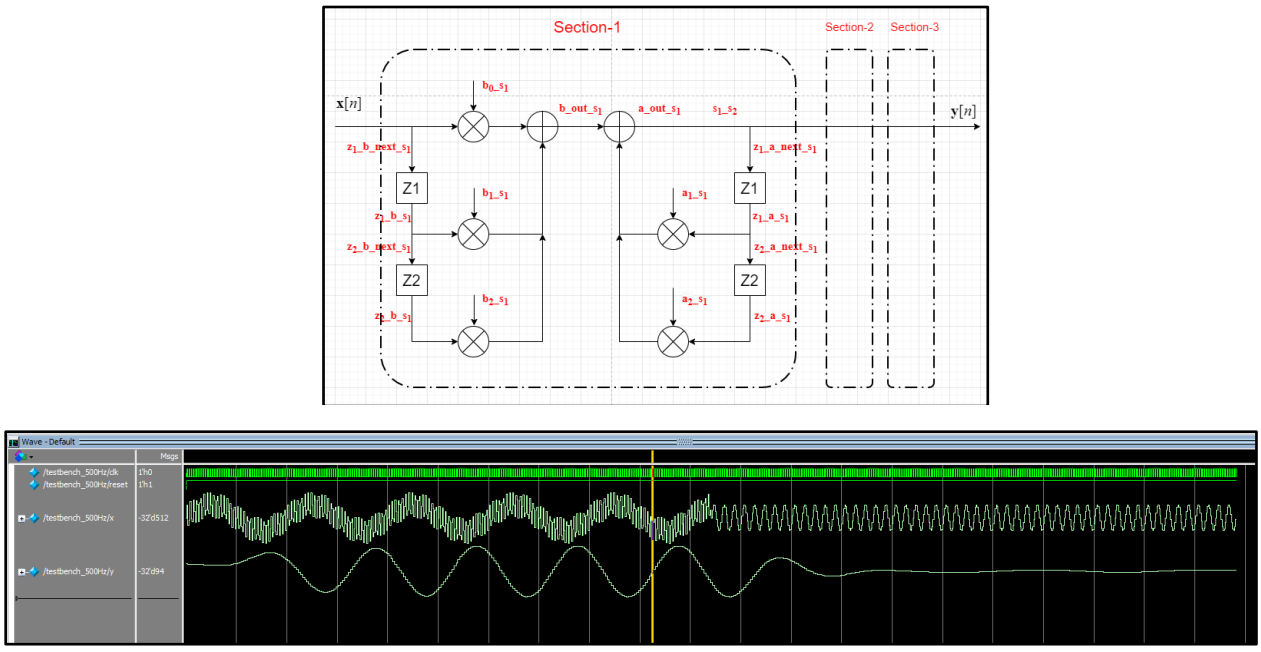


Fig. 2: Design and Implement of IIR Filter

III. Conclusion

We built, studied, and implemented FIR and IIR filters in this paper. Furthermore, Verilog HDL has employed those filter design parameters in hardware implementation. The uniqueness of the proposed digital system design is demonstrated using a visual test-bench. We expect that this study will be useful to researchers working on system on chip research and development.

Acknowledgement

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