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Review of the Ways to Balance the Capacitor Voltages of the Three Level Inverter for Grid Connected Solar PV with BESS

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A B S T R A C T

Renewable energy resources are used to generate energy, which minimises pollution while also boosting economic benefits and maintaining energy security. Increasing the national solar generation capacity to 100 GW by 2022 is a part of India's renewable energy initiatives. Given the country's abundant solar potential, there is a huge chance to harness solar energy. However, in order to reach the 2022 deadline, the rate of solar capacity installation must be greatly increased. Advanced power electronic systems are necessary to use and develop renewable energy sources. The use of maximum power from the source is one of the most important responsibilities of power electronic systems in solar PV or wind energy applications.The three-level ac-side phase voltages are produced by two capacitors on the dc side of the converter. Because unbalanced capacitor voltages have been known to alter ac side voltages and induce unanticipated behaviour on system parameters such as even-harmonic injection and power ripple, the capacitor voltages are usually believed to be balancedusing various methods.This paper goes over the many research that have been done so far in order to improve the coordination of solar PV with battery storage and the system designs that go with it.

Keywords: Solar PV, unbalanced volatges, three level inverter, pulse width modulation.

1. Introduction

Renewable energy sources such as photovoltaic (PV) and wind generation systems are becoming more promising alternative to conventional generation units for electricity generation. To use and develop renewable energy sources, advanced power electronic systems are required. One of the most significant roles of power electronic systems in solar PV or wind energy applications is to utilise maximum power from the source [3]–[5]. To transmit power from a renewable energy resource to the grid in three-phase applications, two types of power electronic designs are usually used:

- **Double-stage conversion** (stage one uses a dc/dc converter to help the PV array's maximum power point tracking (MPPT). whereas, the second stage uses a dc/ac inverter to generate the correct dc voltage for the.)
- **Single-stage conversion** (it requires only one converter to complete the double-stage duties, resulting in a reduced cost and improved efficiency for the system; nevertheless, a more complex control mechanism will be necessary.)

A three-phase, single-stage PV energy system with a voltage-source converter (VSC) for power conversion is now the industry standard for high-power applications [4]. Solar and wind energy systems, on the other hand, are notorious for being unreliable and fluctuating. This problem can be solved by combining grid-connected renewable energy systems with battery energy storage, which can improve power system control flexibility and overall system availability [2]. A converter is typically required to control the charging and discharging of the battery storage system, as well as another converter for dc/ac power conversion; hence, a three phase PV system connected to battery storage will require two converters.

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2. Three-level inverter structure

Three-level inverters have been widely employed in a variety of applications since its inception in 1981, including motor drives, STATCOM, HVDC, pulse width modulation (PWM) rectifiers, active power filters (APFs), and renewable energy applications [7], [8]. A typical three-phase three-level neutral-point-clamped (NPC) inverter circuit is shown in Fig. 2.1(a). The three-level ac-side phase voltages are produced by two capacitors on the dc side of the converter. Because unbalanced capacitor voltages have been known to alter ac side voltages and induce unanticipated behaviour on system parameters such as even-harmonic injection and power ripple, the capacitor voltages are usually believed to be balanced. [7] and [9].

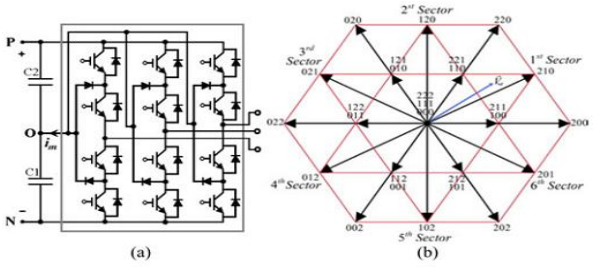

Fig 2.1 Typical three-level inverter (a) structure of circuit (b) three-level inverter

2.1 balanced capacitors voltage

Using modulation algorithms, many solutions for balancing capacitor voltages have been developed, including

- Space vector pulse width modulation (SVPWM) [17] or
- Sinusoidal carrier based PWM (SPWM).

To balance the dc-link capacitors in SPWM applications, most solutions rely on injecting the necessary zero-sequence signal into the modulation signals [12], [13], [16], [18]. In SVPWM applications, a greater knowledge of the effects of switching options on capacitor voltages in the vector space has led to a slew of solutions for balancing capacitor voltages in the three-level NPC inverter. Capacitor balancing with traditional SVPWM, virtual SVPWM (VSVPWM), and their combination are among them. [14], [15], [19].

In vector control theory, the inverter should be able to generate the voltage output immediately while following the control system's reference vector (Vref). However, because to the inverter's switch limitations, it is impossible to guarantee that any desired vector will be formed; in reality, only a limited number of vectors (27 for a three-level inverter) may be generated. To solve these challenges, the reference vector, Vref, is generated in any space vector modulation (SVM) scheme such as SVPWM and VSVPWM by picking the right available vectors in each time frame in such a way that the average of the applied vectors must match the reference vector.

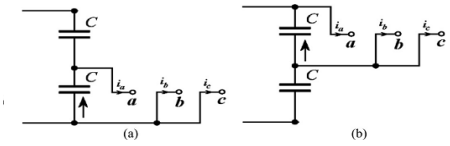

Fig. 2.2 Equivalent circuit and capacitors current with two different short vector.

(a) Short vector—100.

(b) Short vector—211.

Equation (2.1) shows the mathematical relation between the timing of the applied vectors and the reference vector

$$\begin{cases} T_s\vec{V}_{ref} = \sum_{i=1}^{n} T_i\vec{V}_i \quad (1) \\ T_8 = \sum_{i=1}^{n} T_i \end{cases}$$

Ts is the time frame, which should be as short as possible. It can be thought of as a control update phase during which a mathematically derived average vector is generated. The time segment Ti corresponds to the selected inverter vector V_i, and the number of applied vectors is n. In general, the reference

vector is formed by three independent vectors (n=3), and (2.1) can be turned into three different equations with three variables to be calculated: T_1, T_2, and T_3. Several vector PWM algorithms [6], [7], [9]–[11], and [13]–[15] use a similar timing computation technique.

The space vector diagram of a three-level inverter for balanced dc-link capacitors [6] is shown in Fig. 2.1(b). It has 27 switching states from which to choose from 19 different voltage vectors. The switching state of the inverter phases is represented by the number associated with each vector in Fig. 2.1(b). From the inverter ac side, the voltage vectors can be classified into five classes based on their amplitudes and effects on different capacitor voltages. They are

- Six long vectors (200, 220, 020, 022, 002, and 202),
- Three zero vectors (000, 111, and 222),
- Six medium vectors (210, 120, 021, 012, 102, and 201),
- Six upper short vectors (211, 221, 121, 122, 112, and 212), and
- Six lower short vectors (100, 110, 010, 011, 001, and 101).

When one of the selections (Vi) is a short vector, there are two options for generating Vref that will generate the same result on the ac side of the inverter in the three wire connection (if voltages are balanced). On the ac side of the inverter, the short vector "211" will have the same effect as "100."

However, on the dc side, this option will result in the employment of a different dc capacitor for power transfer from or to the ac side, as well as a different capacitor being charged or discharged depending on the switching states and the direction of the ac side current. When "100" or "211" is picked, for example, Fig. 2.2 depicts how the capacitors are connected, indicating how different capacitors are engaged in the power transfer. In most cases, capacitor balance is required.

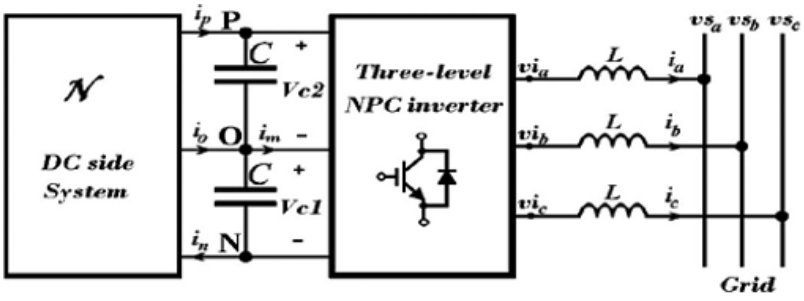

Fig.2.3: General diagram of a grid connected three-wire three-level inverter.

The vector diagram of Fig. 2.1(b) is utilised to generate the ac-side waveform, with the dc capacitor voltages assumed to be balanced. Using the expression given in Fig. 2.1(b), determine the relevant vectors to be picked and compute their related timing (Ti) for implementing the required reference vector (2.1). Despite the control system's best efforts to guarantee balanced capacitor voltages, if any unbalance occurs during a transient or an unanticipated operation, the aforementioned technique may create an erroneous ac-side waveform that may differ from the control system's actual required vector. Even-harmonics, imbalanced current, and unpredicted dynamic behaviour can all emerge from this.

The necessity of balanced capacitor voltages, on the other hand, may be overly limiting in some situations. Working with either balanced or unbalanced capacitor voltages is conceivable. The method suggested in this study is based on the fact that capacitor voltages can be balanced or unbalanced. To fulfil the system's desired objectives, it's critical to be able to construct an accurate reference vector based on (2.1), regardless of whether the capacitor voltages are balanced or not.

2.3. Unbalanced capacitor voltages

Figure 2.3 depicts the general structure of a grid-connected three-level inverter, including the dc and ac sides. Depending on the inverter's application, the dc-side system, denoted by "N," might be built up of a variety of circuit layouts. For example, the dc-side system could be a solar PV system, a wind generator with a rectifying circuit, a battery storage system, or a mix of these systems with differing or equal dc voltage across each capacitor.

The overall view of the switching effects on a three-wire connection of a three-level NPC inverter with a mixture of these systems on the dc side is one of the primary ideas of this work. Mathematically, in a three-wire connection of a two-level inverter, the d_{q0}field,v_d,v_q, and v_0 of the inverter in vector control can be considered as having two degrees of freedom in the control system; because the zero sequence voltage, v_0 will have no effect on the

system behavior in both the dc and the ac side of the inverter. However, in the three-level three-wire application illustrated in Fig. 2.3, with fixed v_d and v_q although v_0 will have no effect on the ac-side behavior, it can be useful to take advantage of v_0 to provide a new degree of freedom to control the sharing of the capacitor voltages in the dc bus of the inverter. It is now able to control and operate the vectors using balanced and unbalanced dc, assuming $V_{c1}V_{c2}$.—

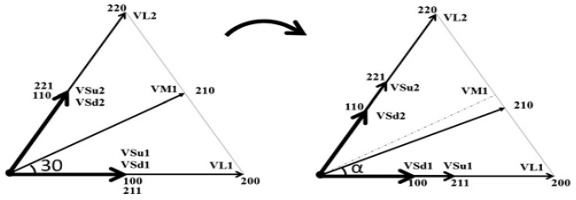

Fig.2.4: vector diagram of balanced and unbalanced capacitor voltage

The vector diagram in the first sector of Fig. 2.1(b) shows how the inverter changes under both balanced and unbalanced capacitor voltages while maintaining the right ac voltages. This feature is especially useful in situations where the two capacitor voltages may differ, such as when connecting two PV modules with different MPPT points, or when connecting a P module across the two capacitors and including battery storage at the midpoint of the two capacitors, or when connecting batter storage to each of the capacitors with the ability to transfer different power from each battery storage.

2.4. Effect of unbalanced capacitor voltages

In the vector diagram shown in Fig. 2.1(b), capacitor voltage unbalance causes the short and medium vectors to have different magnitudes and angles compared to the case when the capacitor voltages are balanced. Fig. 2.4 shows the differences between two cases as highlighted in the first sector of the sextant in Fig. 2.1(b) for$V_{C1}<V_{C2}$.Vector related to the switching state V_I can be calculated as follows [20]:

$$V_1=\frac{2}{3}\left(V_{aN}+\vec{a}V_{bN}+\vec{a}^2V_{cN}\right)^{(2)}$$

Where a=ej(2π 3) and V_{aN}, V_{bN} and V_{cN} are the voltage values of each phase with reference to "N" in Fig. 2.1(a). Assuming that the length of the long vectors ((2/3)V_{dc}) is 1 unit and the voltage of capacitorC_1,V_{c1} =h_V dc,for0≤h≤1, then the vectors in the first sector can be calculated using (2.2) and the results are given in (3)–(9)

$$\vec{V}sd1=h^{(3)}$$

$$\vec{V}su1=1-h^{(4)}$$

$$\vec{V}l1=1^{(5)}$$

$$\vec{V}l2=\frac{1}{2}+\frac{\sqrt{3}}{2}j^{(6)}$$

$$\vec{V}sd2=h\left(\frac{1}{2}+\frac{\sqrt{3}}{2}j\right)^{(7)}$$

$$\vec{V}su2=(1-h)\left(\frac{1}{2}+\frac{\sqrt{3}}{2}j\right)^{(8)}$$

$$\vec{V}m1=\left(1-\frac{h}{2}\right)+h\frac{\sqrt{3}}{2}j^{(9)}$$

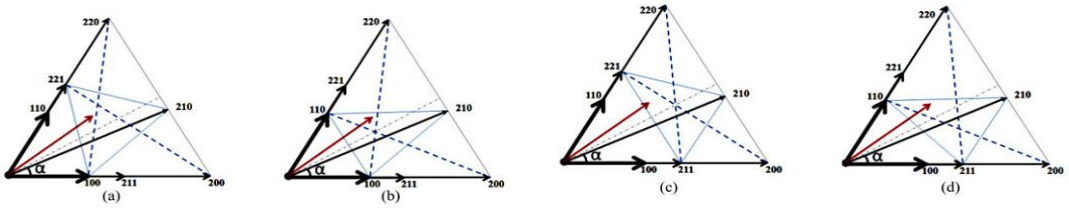

Fig 2.5: Different possible vector selection ideas.

Similarly, the vectors in the other sectors can be determined. The magnitudes and angles of the vectors can be adjusted depending on the capacitor voltages, as shown in Equations (2.3)–(2.9). When h=0.5, for example, the two capacitor voltages are the identical, as are the two short vectors, $V_{sl1}=V_{su1}$. The vectors will have different magnitudes if the two capacitor voltages are different. Because the magnitudes of the short vectors have changed, the selection of these short vectors will now have a different influence on both the dc and ac sides.

Traditionally, each pair of short vectors is considered to be redundant, as the selection of any of the short vectors at any instance will have the same effect on the ac side. However, when the two capacitor voltages are different, the short vectors cannot be considered to be redundant any more. Thus, when h=0.5, each different short vector needs different timing to generate the requested vector based on (2.1).

2.5. Selecting vectors under unbalanced dc voltage condition and their effects on the ac side of inverter

To generate a reference vector based on (2.1), different combinations can be implemented. Fig. 2.5 shows different possible vector selections to generate a reference vector (V ∗) in the first sector based on the selections of different short vectors. For example, to generate V ∗ based on Fig. 2.5(a), one of following combinations can be selected with proper timing based on (2.1). The combinations are:

- (221–210–100),
- (221–220–100),
- (221– 200–100),
- (221–200–Zero),
- (000–220–Zero),
- (220–200–Zero),

Where, “Zero” can be “000” or “111” or “222”. This demonstrates that there is flexibility in choosing the correct vector selections. Although all of these selections with suitable timing can generate the same reference vector, they have different impacts on the dc and ac side of the inverter in their instantaneous behavior.

The correctness of the generated voltage must be investigated in order to evaluate the ac-side behaviour. In order to have the right instantaneous current in the ac side of the system, the requested voltage V (t) should ideally be created exactly and simultaneously in the three phases of the inverter. However, due to the inverter's inadequate ability to provide the precise value of the needed voltage in each phase, only the average value of the requested vector V for the defined time window of T_s can be produced in the short time T_s. To analyse the ac-side voltages' continuous time behaviour, the error vector e(t) can be determined to see how far the generated voltage deviates from the desired vector, as shown below:

$$\vec{e}(t)=\vec{V}^{*}(t)-\vec{V}_{apl}(t) \quad (10)$$

$$E(t)\triangleq\left|\int_0^t \vec{e}(t)dt\right|; \quad 0\le t\le T_8 \quad (11)$$

Where, $V_{apl}(t)$is the applied vector at the time “t”. This error can result in harmonic current across the impedance connected between the inverter and the grid. If this impedance is an inductor then the ripple in the inductors current I_{rL}can be expressed as

$$\vec{I}rL=1/L\int_0^t \vec{e}(t)dt \quad (12)$$

Where e(t) is defined as

$$e(t) \triangleq L\frac{d\vec{I}rL}{dt} \text{ (13)}$$

In order to deduce (2.13), it is assumed that the sought vector V (t) will generate sinusoidal current in the inductor, which is generally acceptable in the system's continuous time behaviour. The absolute value of error e(t) is directly connected to the magnitude of the inductors current ripple, according to (2.11) and (2.12). Although E(Ts)=0, or the sum of errors for the period Ts is zero, it is crucial to decrease the error at each time instant to lower the size of high frequency ripples. The three nearest vectors (TNV) are commonly employed to accomplish this. For example, in Fig. 5(a), the group (221, 210, 100, or 211) appears to be the best three nearby vectors to be picked in the TNV method to construct the needed vector V*.

A smart timing technique for each vector in the TNV approach, such as separating the time to apply each vector into two or more shorter times, has also been proposed to lower e(t). However, switching losses will increase as a result of this. A frequent and appropriate solution is to divide by two. Furthermore, lowering Ts lowers the error e(t) while increasing the accuracy of the control system's requested vector. The accuracy of the requested vector calculation can be increased by reducing the sampling time and the vector calculation time, according to the basic rule of digital control.

2.6 .selecting vectors under unbalanced dc voltage

Conditions on the DC Side of the Inverter and Their Effects Varied vectors have different impacts on the capacitor voltages on the dc side, which are dependent on the sum of the incoming currents from the dc side and the inverter side.

ip, io, and in are dc-side system currents that depend on the dc-side system circuit architecture and capacitor voltages, as shown in Fig. 2.3. The inverter currents are related to inverter switching and the ac side of inverter currents, both of which are directly affected by the inverter's implemented vectors. As described in Chapter 2, different vectors will transport ac-side currents and power to capacitors in different ways.

The instantaneous power transmitted to the dc side of the inverter from the ac side can be calculated as follows:

$$p(t) = \upsilon I_a.i_a + \upsilon Ib. + \upsilon I_c.i_c \text{ (14)}$$

Where v_{Ia}, v_{Ib}, and v_{Ic} are the ac-side inverter instantaneous voltages with reference to the "N" point, and i_a, i_b, i_c are inverter currents. For example, in the first sector of the vector diagram shown in Fig.2. 4, p(t)for the short vectors can be expressed by the following equations:

$$\begin{cases} p211(t) = 1(1-h)Vdc*i_a \text{ (15)} \\ p100(t) = hVdc*(-i_a) \end{cases}$$

$$\begin{cases} p221(t) = 1(1-h)Vdc*(-i_c) \text{ (16)} \\ p110(t) = hVdc*i_c \end{cases}$$

Selecting the top short vectors, "211" and "221," will impact the upper capacitor voltage, while selecting the lower short vectors, "100" and "110," will effect the lower capacitor voltage, ignoring the dc-side system behaviour. When ia > 0, for example, if vector "211" is selected, the higher capacitor will be charged without affecting the lower capacitor voltage, and if vector 100 is selected, the lower capacitor will be discharged without affecting the upper capacitor voltage. The pace of charging and discharging, as well as their dependence on Vdc values and inverter currents, can be studied using (2.15) and (2.16). However, in order to conduct correct research, the dc side system behaviour must be considered in the regulation of capacitor voltage charging and discharging rates.

2.7 The Space Vector PWM Technique

For each PWM cycle, the Space Vector PWM generation module accepts modulation index commands and generates the proper gate drive waveforms. The SVPWM module's operation and configuration are described in this section. A three-phase two-level inverter with dc link architecture can have up to eight switching states, each of which creates the inverter's output voltage. In the Space Vector plane, each inverter switching state yields a voltage Space Vector (V_1 to V_6 active vectors, V_7 and V_8 zero voltage vectors) (Figure2.1 space vector diagram). Each active vector (V_1 to V_6) has a magnitude of 2/3 Vdc (dc bus voltage).

The Space Vector PWM (SVPWM) module inputs modulation index commands (U_Alpha and U_Beta) which are orthogonal signals (Alpha and Beta) as shown in Figure. The gain characteristic of the SVPWM module is given in Figure 2.1. The vertical axis of Figure represents the normalized peak motor phase voltage (V/V_{dc}) and the horizontal axis represents the normalized modulation index (M). The inverter fundamental line-

to-line RMS output voltage (V_{line}) can be approximated (linear range) by the following equation:

$$Vline = Umag * Mod\_Scl * / \sqrt{6} / 2^{25} .....(1)$$

Where dc bus voltage (V_{dc}) is in volts

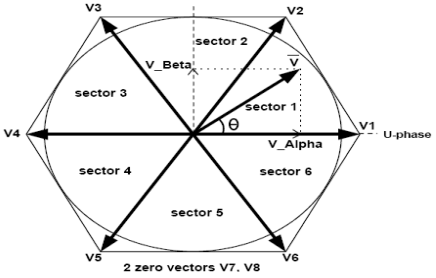

Figure 2.6: Space Vector Diagram

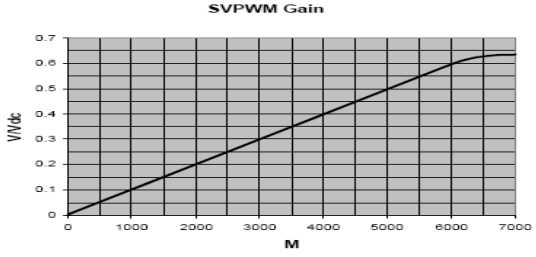

Figure2.7:transfer characteristics

2.7.1 Transfer Characteristics

The maximum achievable modulation (Umag_L) in the linear operating range is given by:

$$Umag\_L = 2^{25} * \sqrt{3} / Mod\_scl .....(2)$$

When modulation Umag>Umag L, overmodulation occurs. This is the condition in which the voltage vector in (Figure: voltage vector rescaling) exceeds the hexagon boundary. In this case, the Space Vector PWM algorithm will rescale the voltage vector's magnitude to fit within the Hexagon limit. The voltage vector's magnitude is limited within the Hexagon, but the phase angle (θ) is always kept. In the overmodulation zone, the PWM modulator's transfer gain (Figure2.7) decreases and becomes non-linear.

2.7.2 PWM Operation

The sub-module SVPWM Tm begins its calculations at the rising edge of the PWM Load signal after receiving the modulation index directives (UAlpha and UBeta). The SVPWM Tm module implements an algorithm that determines the active space vectors (V1 to V6) to be used (based on sector determination) and calculates the appropriate time duration (in terms of one PWM cycle) for each active vector. The zero vectors that are appropriate are also chosen. In overmodulation scenarios, the SVPWM Tm module costs 11 clock cycles on average and 35 clock cycles (worst case Tr) in the worst case. A fresh set of Space Vector timings and vectors is immediately available for actual PWM creation (PhaseU, PhaseV, PhaseW) by sub module PWM Generation at the falling edge of nSYNC. New modulation commands will not be implemented at the earliest PWM cycle unless Pwm Load is triggered at least 35 clock cycles prior to the falling edge of the nSYNC signal. The above Figures voltage vector rescaling

illustrates the PWM waveforms for a voltage vector locates in sector I of the Space Vector plane (shown in Figure). The gating pattern outputs (PWMUH … PWMWL) include dead time insertion.

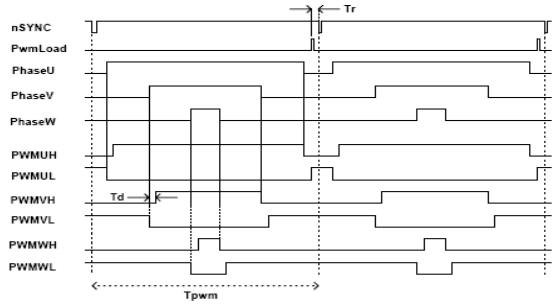

Figure 2.8: 3-phase Space Vector PWM

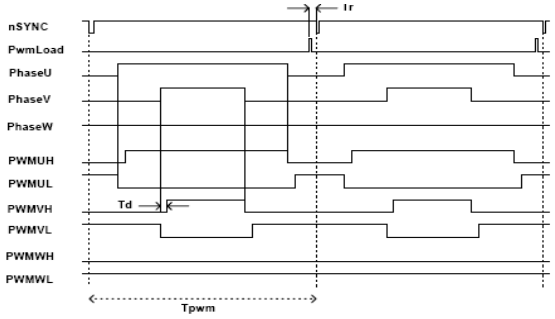

Figure 2.9: 2-phase (6-step PWM) Space Vector PWM

2.7.3 PWM Carrier Period

Input variable PWM Cval controls the duration of a PWM cycle. It should be populated by the system clock frequency (Clk) and PWM frequency (PWM Freq) selection. The variable should be calculated as:

$$PwmCval = ClK\left(2 * PwmFreq\right) - 1 \quad \textbf{(3)}$$

The input resolution of the Space Vector PWM modulator signals U_Alpha and U_Beta is 16-bit signed integer. However, the actual PWM resolution (PwmCval) is limited by the system clock frequency.

2.7.4 Dead Time Insertion Logic

Dead time is inserted at the output of the PWM Generation Module. The resolution is 1 clock cycle or 30nsec at a 33.3 MHz clock and is the same as those of the voltage command registers and the PWM carrier frequency register.

The dead time insertion logic subtracts the amount of dead time from the high side commanded volt*seconds and adds the equal amount of volt*seconds to the low side signal. If the commanded volt*seconds is less than the preset dead time, the full high side turn on pulse is eliminated.

2.7.5 Dead Time Insertion

The dead time insertion logic inserts the programmed dead time between two high and low side of the gate signals within a phase. The dead time register is also double buffered to allow "on the fly" dead time change and control while PWM logic is inactive.

2.8 Sinusoidal Pulse Width Modulation

Sinusoidal Pulse Width Modulation (SPWM), also known as Sine coded Pulse Width Modulation, is used to modulate the inverter output voltage in various industrial applications. The drive's performance is maintained over the whole range of operation, from zero to 78 percent of the value attained by square-wave operation. If the modulation index is greater than this number, the linear relationship between the modulation index and the output

voltage is broken, necessitating the use of over-modulation methods.

2.9 Space Vector Pulse Width Modulation

A different approach to SPWM is based on the space vector representation of voltages in the d, q plane. The d, q components are found by Park transform, where the total power, as well as the impedance, remains unchanged. Fig: space vector shows 8 space vectors in according to 8 switching positions of inverter, V* is the phase-to-center voltage which is obtained by proper selection of adjacent vectors V_1 and V_2.

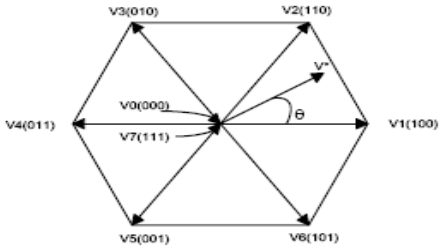

Figure 2.10: Inverter output voltage space vector

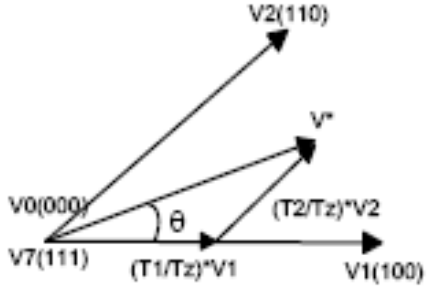

Figure 2.11: Determination of Switching times

The reference space vector V* is given by Equation (1), where T_1, T_2 are the intervals of application of vector V_1 and V_2 respectively, and zero vectors V_0 and V_7 are selected for T_0.

$$V*Tz = V1*T1 + V2*T2 + V0*(T0/2) + V7*(T0/2) \quad (4)$$

Fig.2.12 below shows that, the inverter switching state for the period T_1 for vector V_1 and for vector V_2, resulting switching patterns of each phase of inverter are shown in Fig.2.13 pulse pattern of space vector PWM.

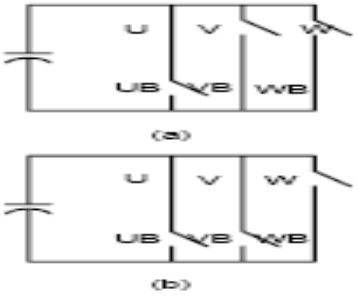

Figure 2.12: Inverter switching state for (a) V1, (b) V2

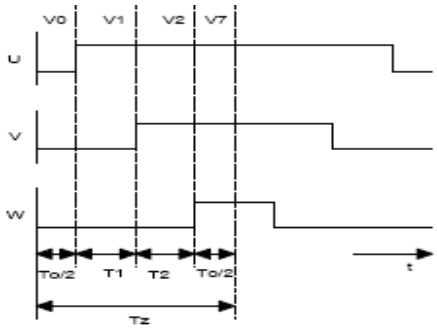

Figure 2.13: Pulse pattern of Space vector PWM

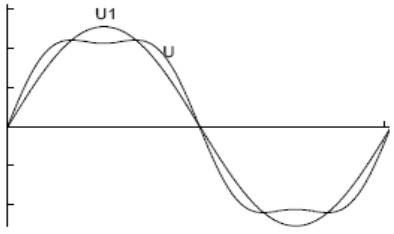

Figure 2.14: Comparison of U and U1

In fig.2.14 comparison U is the phase to- center voltage containing the triple order harmonics that are generated by space vector PWM, and U_1 is the sinusoidal reference voltage. But the triple order harmonics are not appeared in the phase-to-phase voltage as well. This leads to the higher modulation index compared to the SPWM.

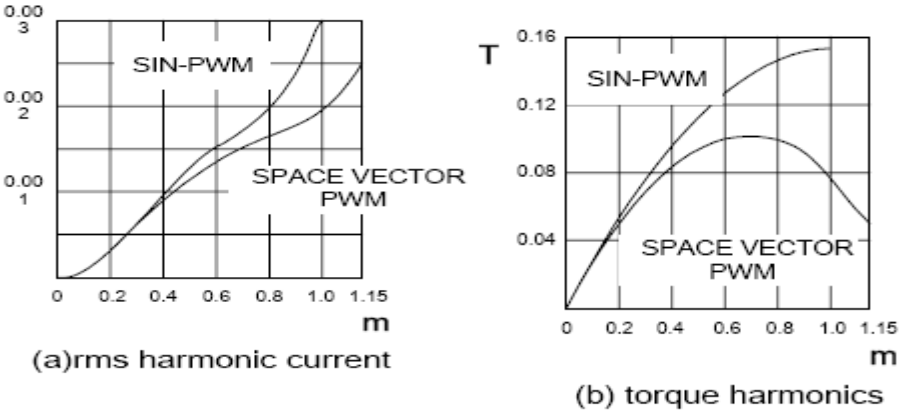

Figure 2.15: comparison of SPWM and space vector PWM (a) rms harmonic current (b)torque harmonic

2.11 SVM PWM Technique

Using the Pulse Width Modulation approach, three phase system voltages can be obtained and applied to the controlled output. The Space Vector Modulation (SVM) approach varies from conventional PWM methods in that it generates all three inverter drive signals at the same time. In digital systems, the SVM process needs less operation time as well as less programme memory.

The SVM algorithm is based on the principle of the space vector u*, which describes all three output voltages ua, ub and uc :

u* = 2/3 . (ua + a . ub + a2 . uc) ……(5)

Where a = -1/2 + j. v3/2 We can distinguish six sectors limited by eight discrete vectors u0…u7 (fig:- inverter output voltage space vector), which correspond to the 2/3 = 8 possible switching states of the power switches of the inverter.

2.12 Space Vector Modulation

The amplitude of u0 and u7 equals 0. The other vectors u1…u6 have the same amplitude and are 60 degrees shifted. By varying the relative on-switching time Tc of the different vectors, the space vector u* and also the output voltages ua, ub and uc can be varied and is defined as:

ua = Re (u*)

ub = Re (u* . a-1)

uc = Re (u* . a-2) ……(6)

During a switching period Tc and considering for example the first sector, the vectors u0, u1 and u2 will be switched on alternatively. Depending on the switching times t0, t1 and t2 the space vector u* is defined as:

u* = 1/Tc . (t0 . u0 + t1 . u1 + t2 . u2)

u* = t0 . u0 + t1 . u1 + t2 . u2

u* = t1 . u1 + t2 . u2 …….. (7)

Where

t0 + t1 + t2 = Tc and

t0 + t1 + t2 = 1

t0, t1 and t2 are the relative values of the on switching times.

They are defined as: t1 = m.cos(a + p/6)

t2 = m.sin a

t0 = 1 - t1 - t2

Their values are implemented in a table for a modulation factor m = 1. Then it will be easy to calculate the space vector u* and the output voltages ua, ub and uc. The voltage vector u* can be provided directly by the optimal vector control laws w1, v_{sa} and v_{sb}. In order to generate the phase voltages ua, ub and uc corresponding to the desired voltage vector u* the following SVM strategy is proposed.

3. Conclusion

Comparison of S-PWM and Space Vector PWM

As mentioned above, S-PWM only reaches to 78 percent of square wave operation, but the amplitude of maximum possible voltage is 90 percent of square-wave in the case of space vector PWM. The maximum phase-to-center voltage by sinusoidal and space vector PWM are respectively

$V_{max} = V_{dc}/2$: Sinusoidal PWM

$V_{max} = V_{dc}/\sqrt{3}$: Space Vector PWM

Where, V_{dc} is DC-Link voltage.

This means that Space Vector PWM can produce about 15 percent higher than Sinusoidal PWM in output voltage.

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